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INFRARED SENSOR READOUT DESIGN

Texas Instruments Incorporated
Equipment Group
P.O. Box 6015, M/S 406
Dallas, Texas 75222

November 1975

Technical Report AFAL-75-149

Final Report for Period 24 June 1974 - April 1975

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
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WRIGHT-PATTERSON AIR FORCE BASE, OHIO

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A conceptual design of a CCD image buffer module for the common-module FLIR has been defined. The image buffer is a solid-state replacement for the electro-optic multiplexer to be used in FLIR systems requiring remote display. This is achieved by loading and storing a field of video signals generated by the parallel-scanned detector array into an analog memory composed of CCDs, then dumping individual lines of video signal out to a CRT as needed. Data and specifications for current modules have been used in conjunction with data and recent technology developments of CCDs to define the image buffer and project the improvements relative to the electro-optic multiplexer. While the image buffer module has been shown to provide benefits in performance, cost, weight, volume and power, the main benefit is in the flexibility of its solid-state configuration as compared with the mechanical complexity of the E-O unit.

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PREFACE

This research was sponsored by the Air Force Avionics Laboratory under Project Number 2004, Task 02, and was performed by Texas Instruments Incorporated, 13500 North Central Expressway, Dallas, Texas 75222, under Contract F33615-74-C-1202. The Air Force program monitor was Edward J. Susedik (AFAL/AFAL/RWI). The research period was 24 June 1974 to 30 April 1975, with the final report being submitted by the authors on 1 August 1975.

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LIST OF APPREVIATIONS

BCCCD	Buried Channel Charge Coupled Device
CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
CTE	Charge Transfer Inefficiency
DLM	Demultiplex-Linear-Multiplex
E-O	Electro-Optics
FLIR	Forward Looking Infrared
LED	Light Emitting Diode
LRU	Line Replaceable Unit
LT	Level Translator
MRT	Minimum Resolvable Temperature
MTF	Modulation Transfer Function
PC	Printed Circuit
SCCCD	Surface Channel Charge Coupled Device
SPS	Series-Parallel-Series
TICAS	Time Interval Compression Addressed Sequentially
TTL	Transistor-Transistor Logic

SECTION I
INTRODUCTION

Infrared raster scan sensors (FLIR) have demonstrated great utility in a wide variety of applications ranging from man-portable to high-performance reconnaissance systems. A major thrust in the FLIR area over the last three years has been the development of common modules as LRUs for a total FLIR system. Use of the modules means that any one of the entire range of applications can be satisfied with one basic set of units with the addition of one custom unit; an afocal optical system. Technology improvements should, however, be made and incorporated into the common modules whenever improvements can be made in the areas of size, weight, power, reliability, cost, performance and flexibility. The application of charge-coupled device (CCD) signal processing to the common module FLIR is expected to produce significant improvements in the areas above. This will be achieved through the replacement of the electro-optic multiplexer with a 100 percent solid-state CCD image buffer module. This module will be used with other common modules to build any FLIR system requiring remote TV display.

The scope of this program was the conceptual layout of a CCD image buffer module for the common module FLIR. Data and specifications for the current modules has been used with data and recent CCD technology developments to define the CCD image buffer and project the improvements relative to the electro-optic multiplexer. All decisions have been based upon demonstrated CCD performance and designs.

The first major factor was the selection of the demultiplex-linear-multiplex (DLM) architecture over other CCD architectures such as serial-parallel-serial (SPS) and linear. The decision was based upon a consideration of performance, interface circuitry and packing density. The total question of packing density has also been treated extensively since the module must be compatible to an EIA standard 525-line CRT independent of the number of detector channels used in the FLIR focal plane. The result is an analog memory organization which is highly versatile with the same PCBs containing the CCDs being used in any modular application. The only changes in the unit from application to application will be the number of memory PCBs used and switches in the overhead circuitry.

Final performance criteria have been evaluated primarily for two-way scan effects in which it has been assured that there will be no perceptible effects at the display from field to field of the CRT. To achieve this, special clocking events are required in the overhead control system, and the CCD must have a dark current of less than 2.5 nA/cm^2 and charge-transfer efficiency of greater than 0.99993. The dark current rating is for 23°C and provides full operation at 54°C.

Other factors such as reliability, maintainability, system safety and design to cost have been evaluated. In all instances the solid state unit has been projected as an excellent module candidate.

SECTION II

SYSTEM APPLICATIONS OF CCD IMAGE BUFFERS

A. CONCEPT

The purpose of the image buffer is to store the parallel output of many infrared detectors for sequential readout in a TV-compatible format. The image buffer would replace the electro-optic multiplexer of the present modular FLIR.

In this present modular FLIR concept, a representation of the infrared scene is created by modulating a light-emitting diode (LED) array with the video from the infrared detector array. The elements of the LED array are connected to those of the detector array in a one-to-one fashion. A visible scene is painted with the LEDs, using the back surface of the receiver scan mirror as shown in Figure 1. TV compatibility is then obtained by viewing the visible scene with a vidicon.

Implementation of the image buffer concept in a FLIR system is shown schematically in Figure 2. The signal from each detector is ac-coupled to a preamplifier and filter. The signals are then loaded simultaneously into the memory units of either one of two memory banks (A or B) during one scan of the mirror (1/60th second). During the next scan, the memory units of the other bank are loaded in a similar fashion while the first-band units are read out sequentially into a video amplifier for immediate display. The sequential readout occurs in about the time of the simultaneous read-in. Therefore, each memory unit is read out at a much higher rate than it

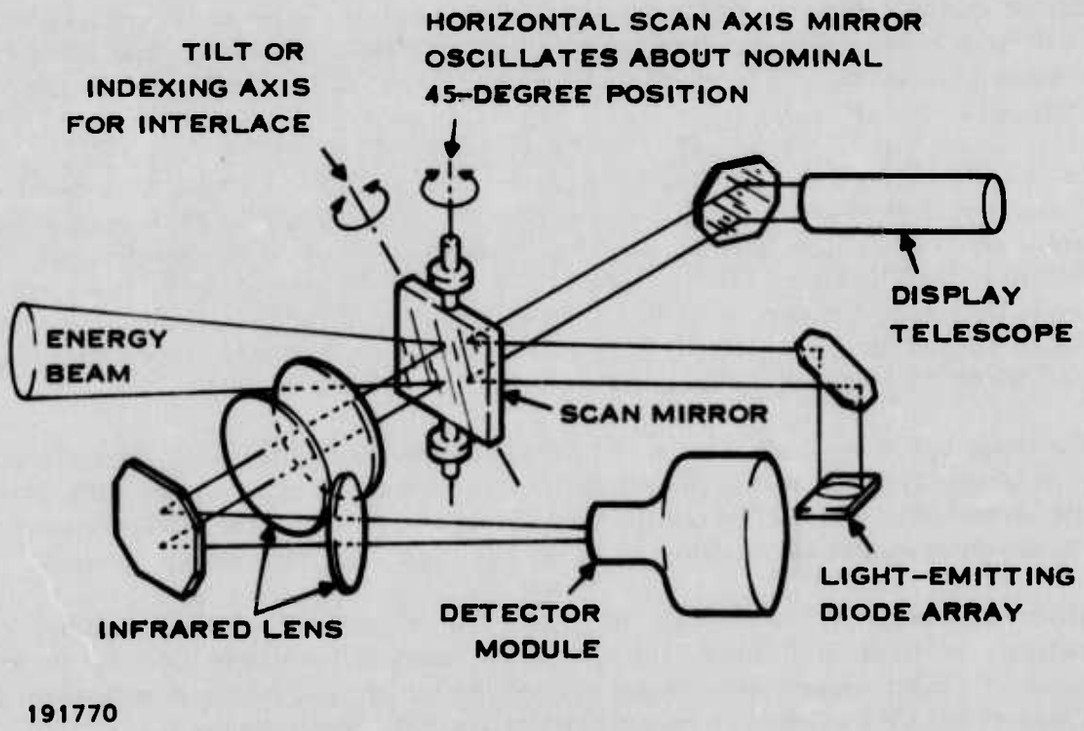

Figure 1. Schematic of Modular FLIR Scan Concept

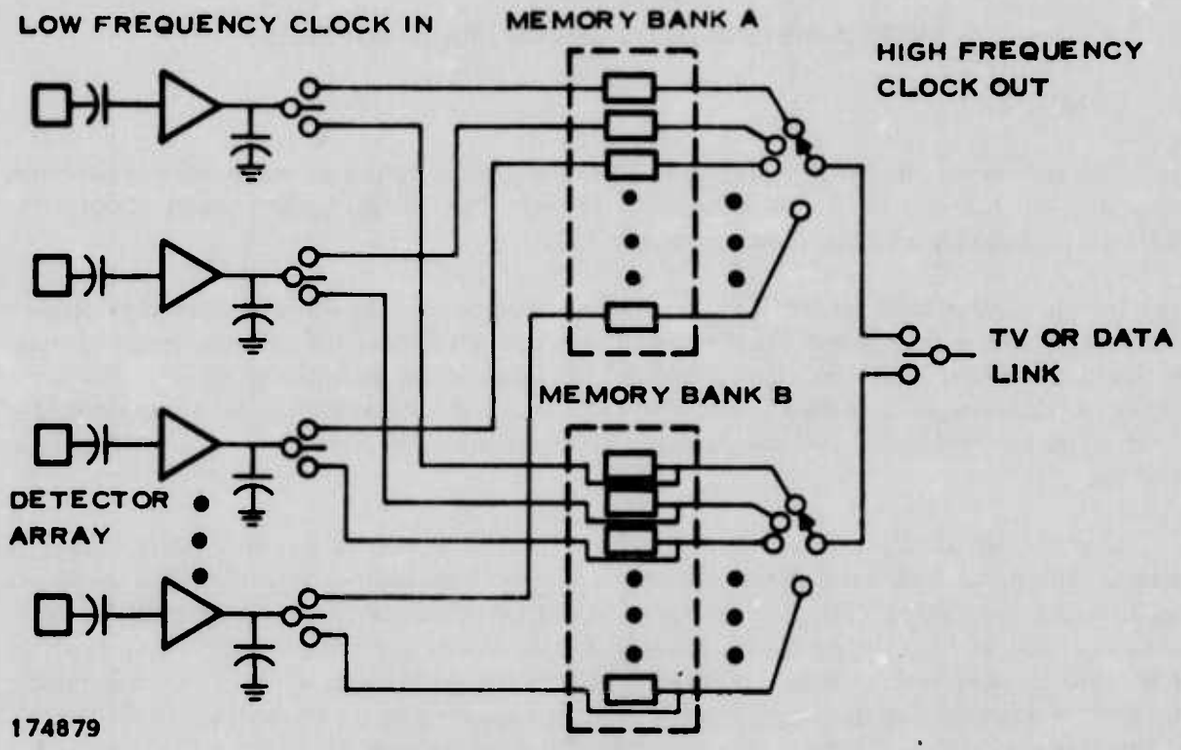

Figure 2. Functional Layout of Image Buffer

is loaded. As shown in Figure 3, the shortest storage time occurs for the last information bit in the first image line, and the longest time occurs in the first bit of the last image line, which is in storage during most of the 1/60th-second mirror scan and most of the 1/60th-second write time of one interlaced video field.

In order to obtain maximum scan efficiency the modular FLIR uses both the forward and reverse directions of the oscillator mirror scanner. The information from the FLIR video chain is both loaded into and dumped from the elements of Bank A in the CCD forward direction. This is referred to as the FIFO mode (First-In-First-Out). In Field B the oscillating mirror is sweeping the scene in the reverse direction while the CRT must still write in the forward direction. Hence, the CCDs of Bank B operate in the LIFO mode (Last-In-First-Out). This is shown schematically in Figure 2 where the input and output nodes of the CCDs are the same points.

The image buffer will replace several modules of the modular FLIRs which require remote display. As shown in Figure 4, the minimal number of replaced elements are the LED drivers, the LEDs, visible optics and the TV camera. Long-term goals not considered within the scope of this particular effort include incorporation of all the video chain into the memory elements.

Within the image buffer module itself are the subunits of control, memory, and postconditioner as shown in Figure 5. The control unit provides the timing trains for clocking the samples of analog imagery data in and out of the buffer, and interfaces with both the infrared scanner and CRT to maintain proper synchronism in the read/write cycle.

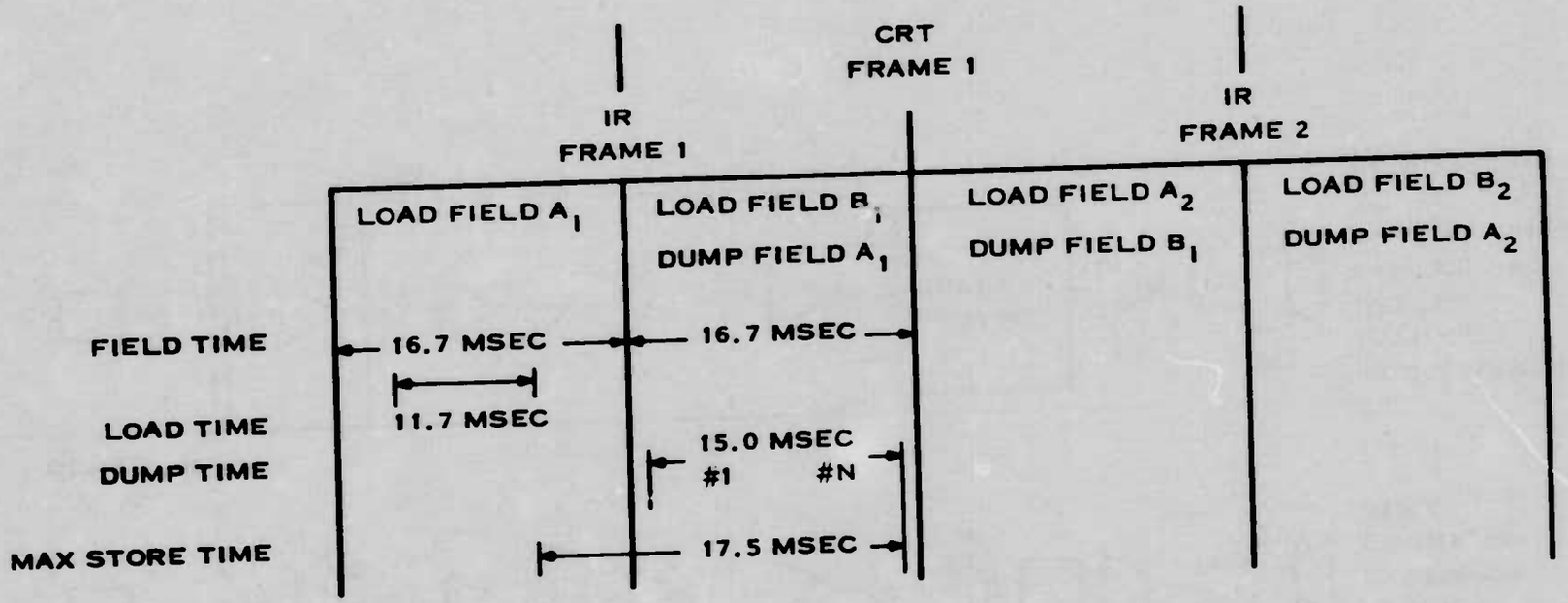

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Figure 3. Image-Buffer Timing

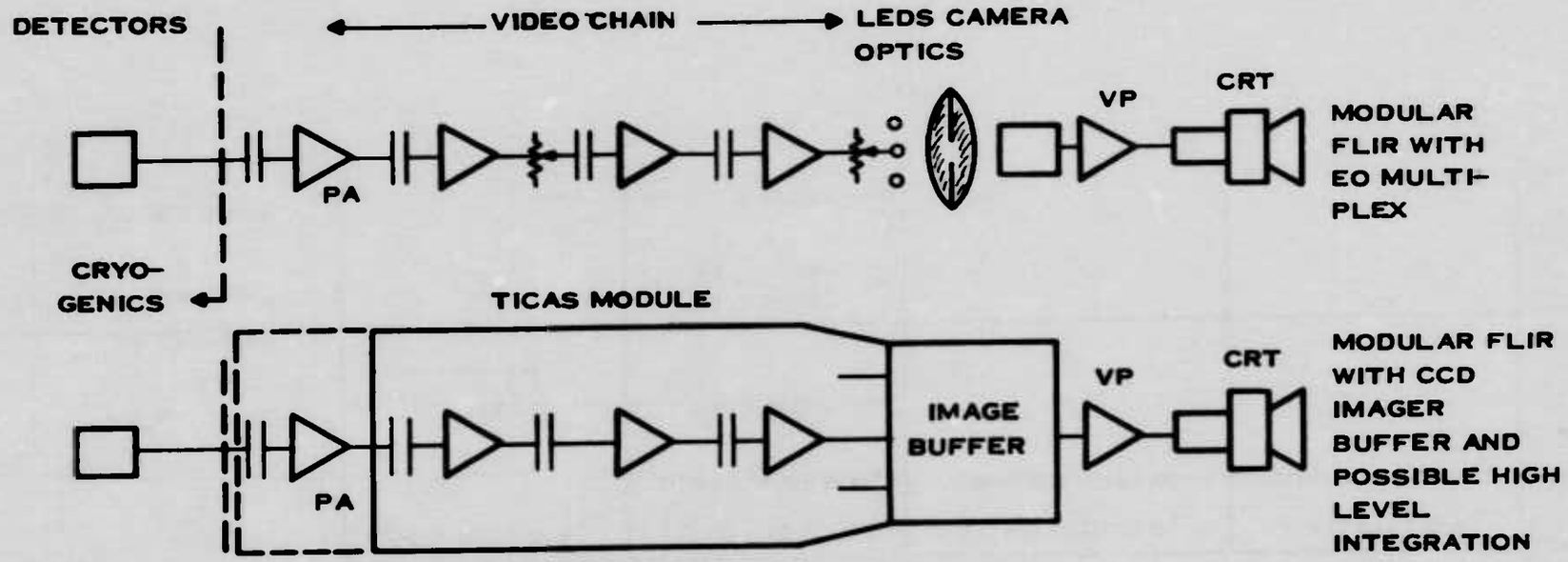

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Figure 4. Near-Term High-Level Integration

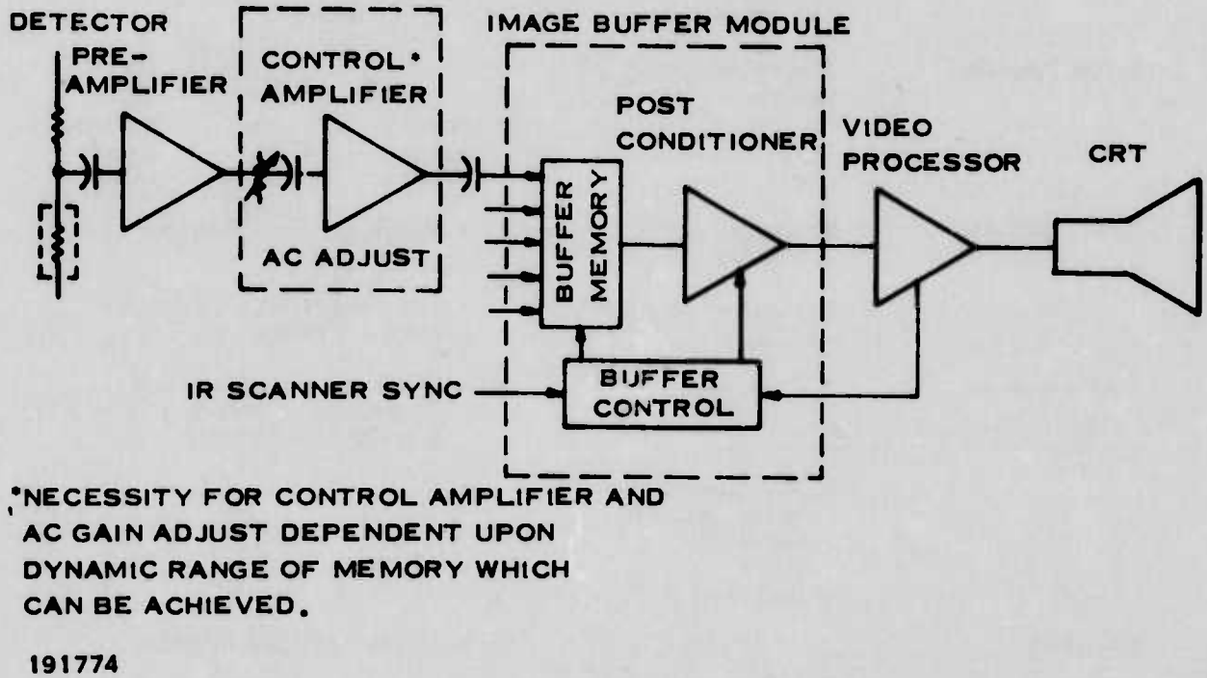

Figure 5. Block Diagram of CCD Image-Buffer Module and Video Chain

The second unit in the buffer is the memory, consisting of PCBs which contain the CCD memories as well as their clock drive buffers and signal-routing logic.

The third unit in the buffer is the postconditioner, which conditions the sampled signal prior to the TV display. The CCD memory units have different ac and dc operating characteristics, just as do the detectors and LEDs. Hence, variations between elements of the memory unit are compensated to present a uniform display response.

B. GOALS AND BENEFITS

The primary goal of the CCD image buffer program is to develop an improved unit which replaces the E-O multiplexer system for converting parallel channels of video to a single line of video for remote CRT display. The module will be completely solid state as compared to the combination of electronic, optical and mechanical parts of the E-O multiplexer. Benefits of the module are itemized in an overview form in Table 1.

Of all benefits listed in the table, items covered by a loose classification of flexibility have the highest impact. These items include the electronic magnification and those under intangibles. The manner in which improved flexibility will be felt is that the cost advantages of the modules can be easily achieved, independent of the application or geometrical constraints placed upon the FLIR.

The specific design goals for modules are given in Table 2. These goals will be referred to during the relevant portions of this report.

TABLE 1. REQUIREMENTS AND ANTICIPATED BENEFITS OF IMAGE BUFFER MODULE

	Requirements	Benefits	
		E-O Multiplexer	CCD Buffer
System Parameters	Lower power, weight and volume		
Power		37 watts	10.3 watts
Volume		330 in^3	284 in^3
Weight		12 lbs.	6.8 lbs.
TV Compatibility	• Interface to EIA Standard 525	• Applicable to any IR imaging system	
	• Electronic magnification	• Filled display independent of the number of IR lines	
System Response	• 2-way scan	• With 2-way scan approximately 30 percent improvement in system MTF at resolution frequency	
	• Approximately 2 samples per resolution element		
	• High device MTF		
Intangibles	———	• Simpler packaging constraints	
		• Solid-state reliability and maintainability	
		• Automatic gain normalization on single line video	
		• High utility in all airborne and shipboard systems and some vehicular systems	

TABLE 2. DESIGN GOALS OF CCD IMAGE BUFFER MODULE

Large area uniformity $< \pm 1$ gray shade
Line-to-line uniformity $< \pm 1/2$ gray shade
No fixed pattern noise
Automatic gain normalization
Standard 525 line CRT
Minimal operating temperature range: $-54°C$ to $+55°C$
Possible operating temperature range: $-54°C$ to $+72°C$
Vibration hardened
Size: 4 by 4½ by 10 inches
Power <8 watts

C. SUBUNIT FUNCTIONS AND PERFORMANCE IMPACT

When analyzing the CCD image buffer in terms of functions and performance, the CCD impact must be considered as an analog sampling element. This can be significant in light of aliasing of both signal and noise. The input to a CCD as used in the image buffer program performs a delta point sampling operation. Hence, both the signal and the noise will be folded about the sampling frequency as shown diagramatically in Figure 6. In the FLIR systems, system resolution frequency is defined in terms of spatial frequency as

$$f_o = 1/[2\ (\Delta\theta)]$$

where $(\Delta\theta)$ is the angular subtense of the square detectors. This means that in an idealized case the system modulation is zero at $2f_o$ while the noise spectra prior to the multiplexer or reformater is limited only by the electronic bandwidth.

When the FLIR video is sampled at a rate of two samples per resolution element, i.e., $4f_o$, no signal aliasing will occur. Noise will, however, be aliased and, as shown in Figure 6, the impact of noise aliasing will be greater at the higher frequencies. If the sampling frequency is reduced, not only will the aliased noise increase, but signal aliasing will also start to occur. At the display level this means that sharp edges could appear twice with possible polarity inversion. An increase in sampling frequency removes the signal aliasing and also reduces the noise aliasing at the expense of increasing the required storage capacity.

- INPUT IS A DELTA POINT SAMPLER – OUTPUT IS A HOLD SIGNAL (DUTY CYCLE ~ 50%)
- SAMPLING FOLDS NOISE AND POSSIBLY SIGNAL BACK INTO DISPLAY
  - SAMPLING RATE (NUMBER OF SAMPLES PER RESOLUTION ELEMENT)
  - ANTI-ALIASING FILTER

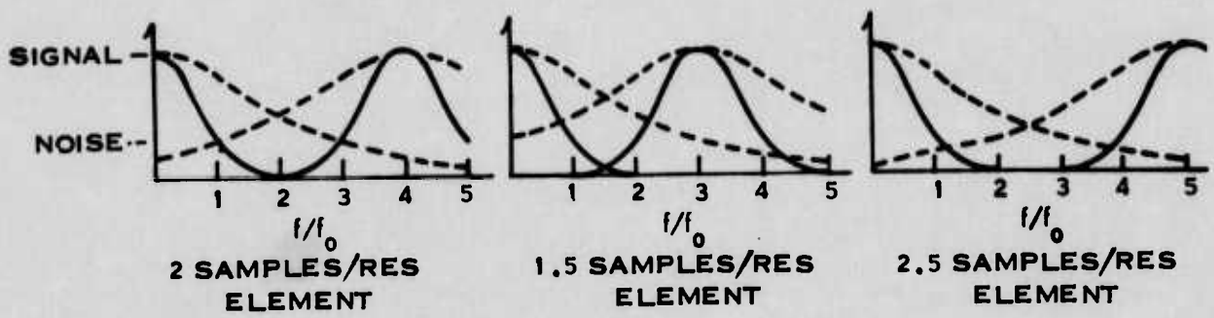

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Figure 6. CCD Sampling Process

In the various parts of Figure 7 are shown the MTF(F) plots for the various elements in the FLIR signal chain, along with frequency plots of the noise amplitude spectrum and the S/N function after each element in the chain. The noise spectrum at the detector consists of white noise plus a 1/f component. Note here that the MTF of the post-CCD peaking amplifier can be chosen to compensate for all the MTF rolloff between the detector output and the sampler at the CCD input. Thus, the noise spectrum at the output of the peaking amplifier is nearly the same as at the detector output. The main source of unrecoverable loss of S/N is in the noise aliasing by the sampling process.

The ideal solution for the aliasing problem is to sample the video at $4f_0$ and incorporate in each channel prior to the CCD, a perfect filter whose cut-off frequency was $2f_0$. The number of components for even a crude approach to a sharp low-pass filter is excessive when it is remembered that this must be done for each IR channel. Hence, in reality, what must be used is something on the order of a simple two-pole filter. The desired effect is to rolloff the noise in the region of $2f_0$ to $4f_0$ but it also decreases both the signal and the noise in the region of 0 to $2f_0$. This loss in modulation however can be recovered in the post-CCD peaking amplifier. The net effect is no degradation in the signal due to the processing electronics and only slight increase in the noise spectrum.

A detailed analytical model for the MRT effects is given in Appendix B and the exact values associated with each subunit of the buffer are discussed in their respective sections.

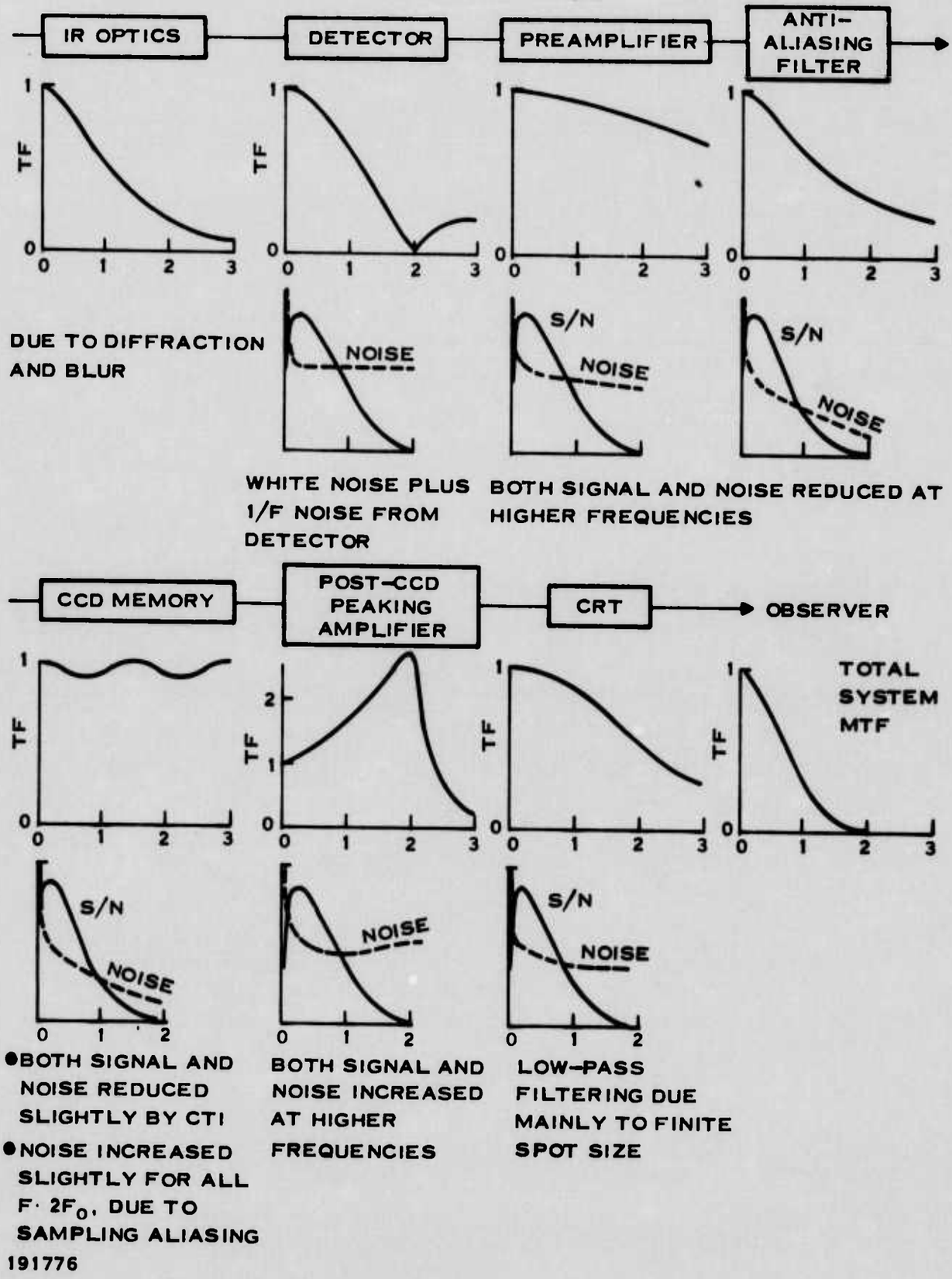

Figure 7. Spectrum of Noise and S/N in the FLIR Image-Buffer Signal Chain

SECTION III
MEMORY ELEMENT

In this section various types of CCD analog memories will be discussed, tradeoffs performed and an optimum memory element specified. This final device specification will result from considerations of system performance, device controls and total interface. For these reasons, discussions of device types must include some assumptions as to the nature of the overhead control circuitry and device functions such as input sampling and output precharge. These assumptions are all discussed in later sections of the report after the DLM has been shown to be the optimum analog memory device for a CCD image buffer.

A. CCD MEMORY

1. Types of Architectures

Three basic CCD geometries were considered in this design study, as shown in Figure 8, linear, serial-parallel-serial (SPS), and demultiplex-linear-multiplex (DLM). In present and future FLIR systems a large number of storage cells are required for each memory unit. Since the MTF of the device depends upon the total number of storage cells that a sample must move through, the linear geometry gives very poor performance.

The SPS array, as configured for consideration in this program, is shown in B, Figure 8. At the start of read-in, the first 30 data elements are clocked into the input serial register. Then they are all shifted down one row into the top positions in the parallel array, and the next row of data elements is clocked in. In this way the parallel array is filled with 900 data elements. During readout these rows of data elements in the parallel array are shifted down in turn to the output serial register and from there clocked out to the output circuit. Thus, all 900 elements are read out in the same sequence in which they are read in.

As expected, this device gives the highest performance. On the other hand, the DLM geometry has a simple drive circuit and requires less power for device operation than does the SPS. Initially, while the device technology was still low and individual cell characteristics were poor, performance requirements demanded that SPS geometries be used. However, as device technology has improved, MTF for the DLM geometry appears to be satisfactory, so that using this geometry conserves cost and power.

2. SPS Array

Figure 9 is a photomicrograph of a typical CCD package used for an SPS breadboard demonstration. It consists of the SPS array itself, on a chip with various other circuits that are not currently being used, and additional chips with the discretes that are used in the output circuit, namely, a sinking resistor for the source follower and an emitter-follower transistor. The functions of the various connection points to the package are given by the lavels around the perimeter of the CCD-package line drawing in Figure 10. The SPS array alone is shown in more detail and at a higher magnification in Figure 11. The input, output and control functions are shown schematically in Figure 12. The control lines shown here are appropriate for the CCDs that are read into during the [field] interval, and from which data are written out at some time during the interval when [$\overline{\text{field}}$] is true.

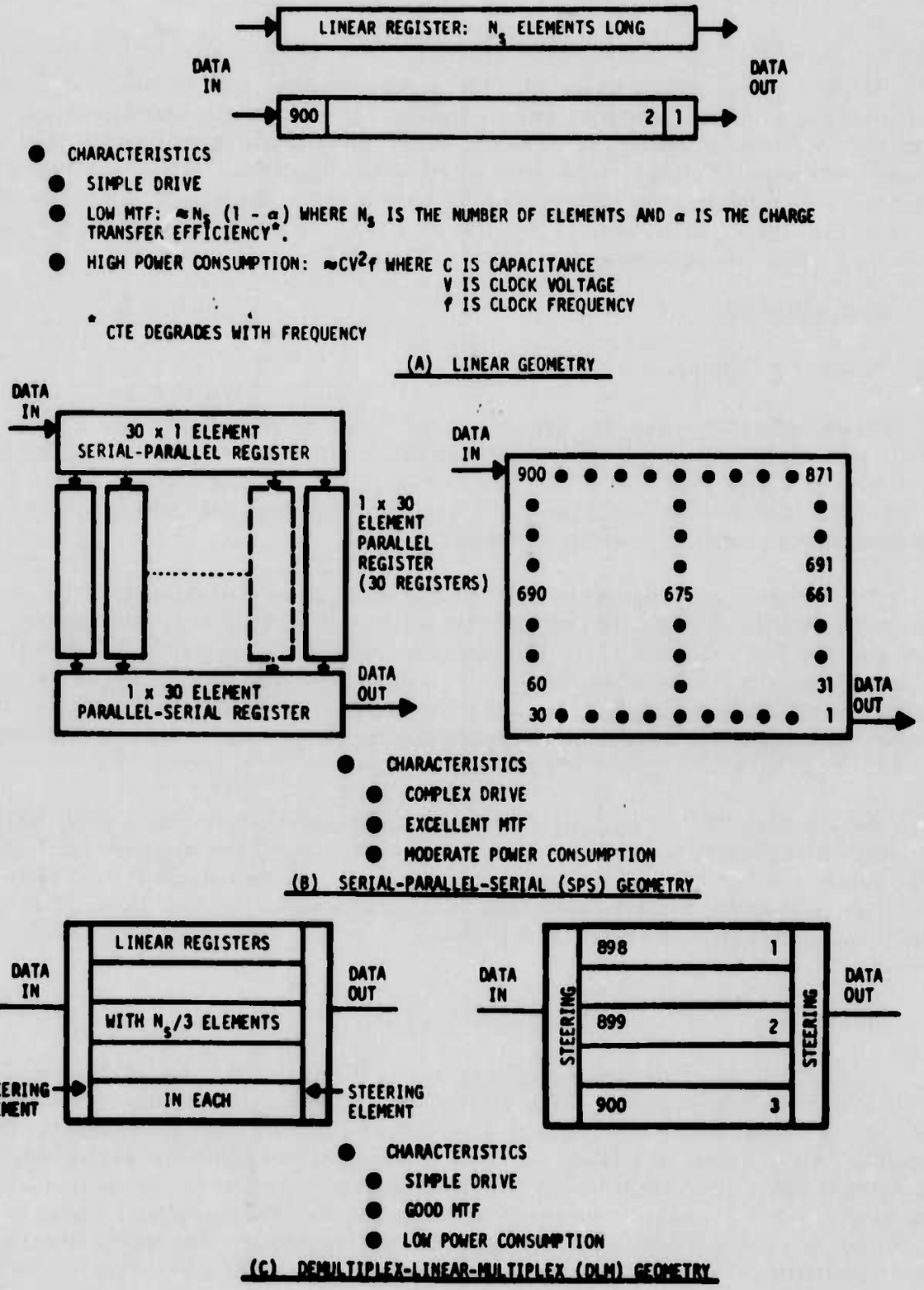

Figure 8. Basic CCD Geometries

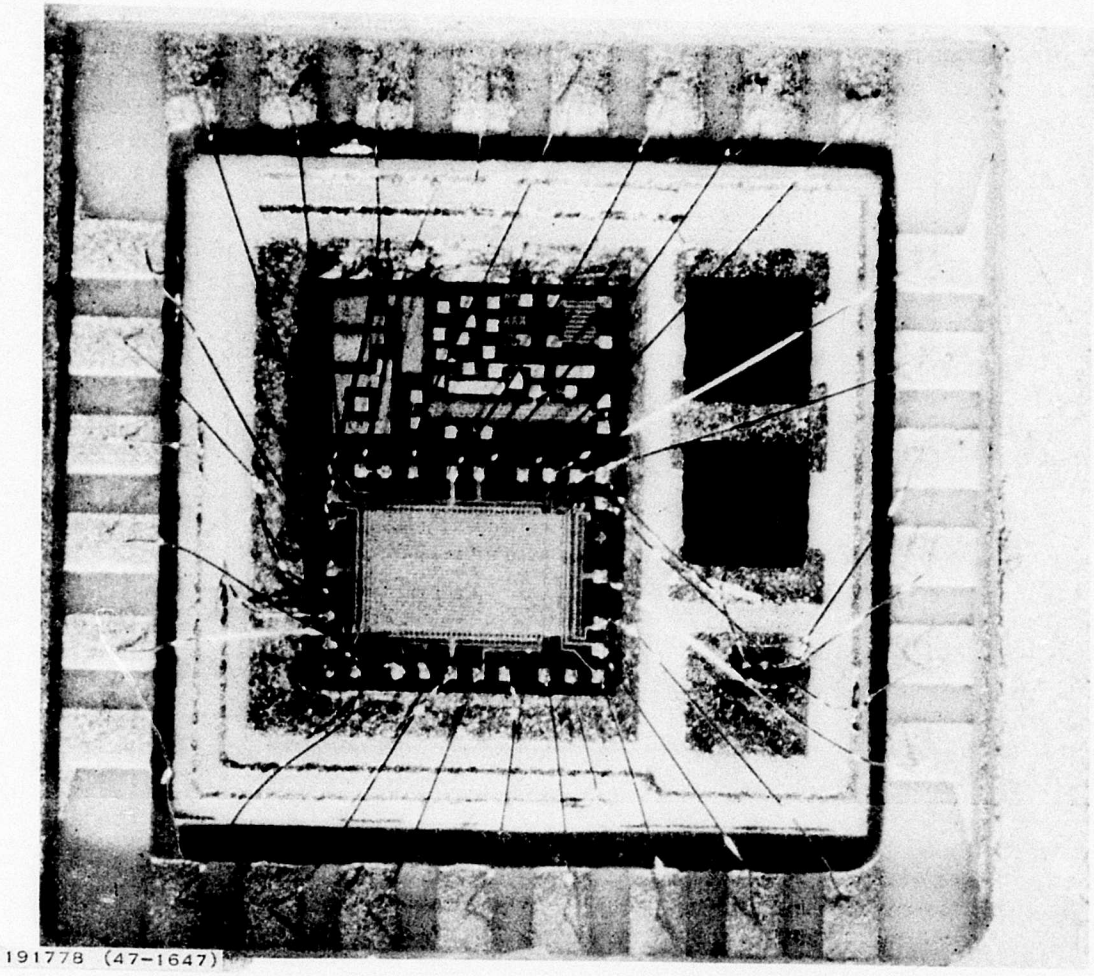

Figure 9. Photomicrograph of a Typical CCD Package: SPS-Type CCD Chip Plus Discrete Elements

Here [field] refers to the high or "true" state of a logic line by which first one subarray of CCDs [bank A] and then the other [bank B] is selected for readout, during the alternate fields of each frame of the TV display. Bank A is selected for readout by the logic state [field], while Bank B is selected by the off-state of [field], i.e., [$\overline{\text{field}}$]. Thus, Figure 12 is appropriate for bank B of CCDs. Note further that only the on-states [board] and [line] are used in further multiplexing individual CCDs of each bank for readout in sequence.

In Figure 12, the sequence of events during read-in starts with the sampling pulse sampling the input signal on the video input line. The amplitude of the sampled signal is converted into a quantity of charge in a charge packet, and this is shifted into and through the upper serial register by the 4-phase slow serial clock. This clock appears on the input clock line only during the read-in interval, which is determined by inputs from the FLIR scan mirror and is generally

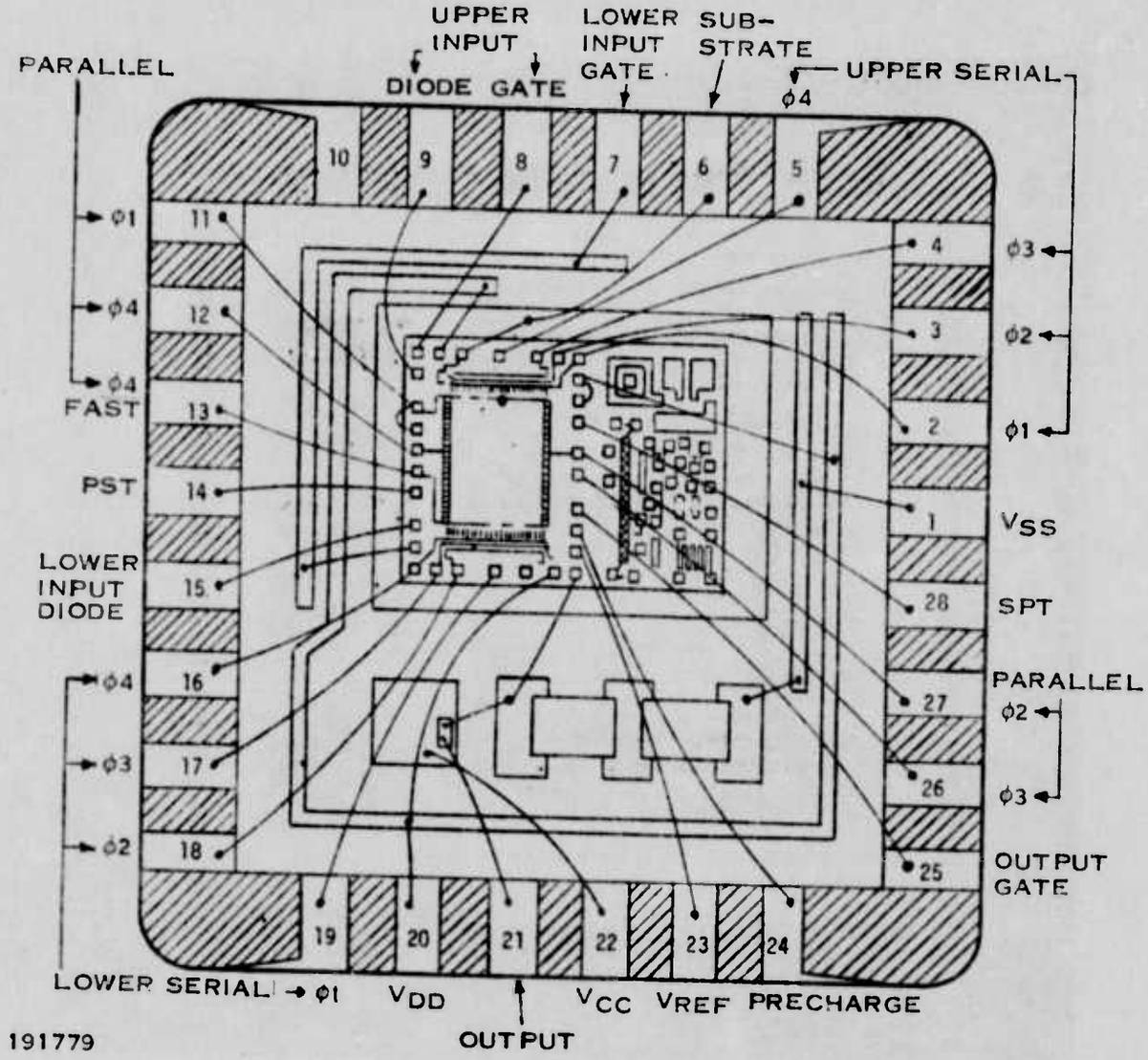

Figure 10. Line Drawing of CCD Package

somewhat shorter than the vertical unblanking interval. In addition, the logical "and" with the [field] line restricts this clock to the read-in intervals for this CCD. When the upper serial register has been filled, the slow serial-to-parallel transfer pulse shifts the set of 30 charge packets in this register to the corresponding storage cells in the first row of the parallel register. Each row of charge packets in the parallel register is transferred in stages to the next lower row by the action of the 4-phase slow parallel clocks, while the next row of charge packets is being assembled in the upper serial register.

During the interval since the last previous readout, dark current has been accumulating in the storage cells of the parallel register. As the rows of signal charge packets are clocked downward in the parallel register, these packets of dark current are swept along ahead of the signal charge packets. As each of these rows of dark current packets reaches the bottom of the

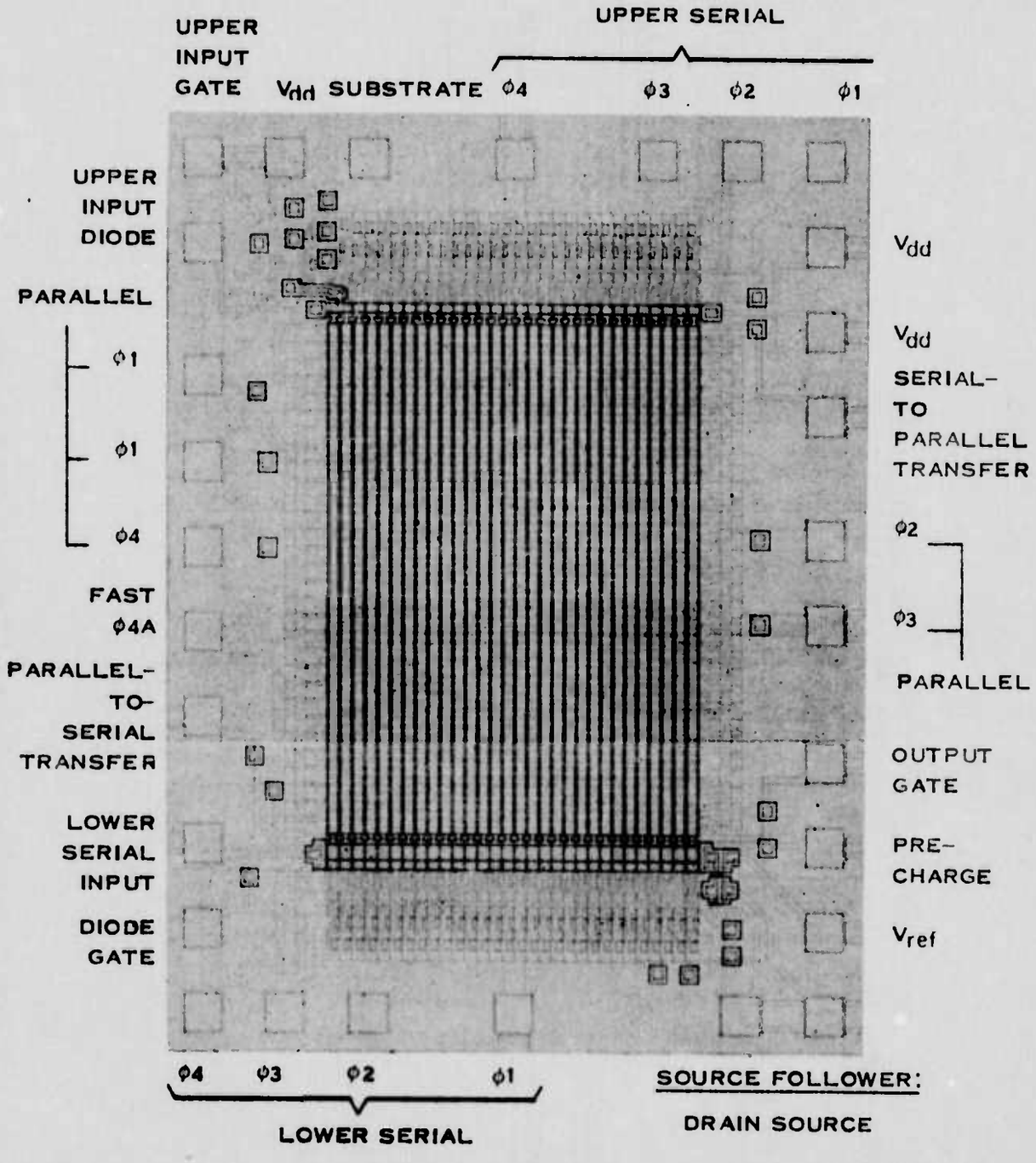

Figure 11. The SPS CCD Array and Its Terminals

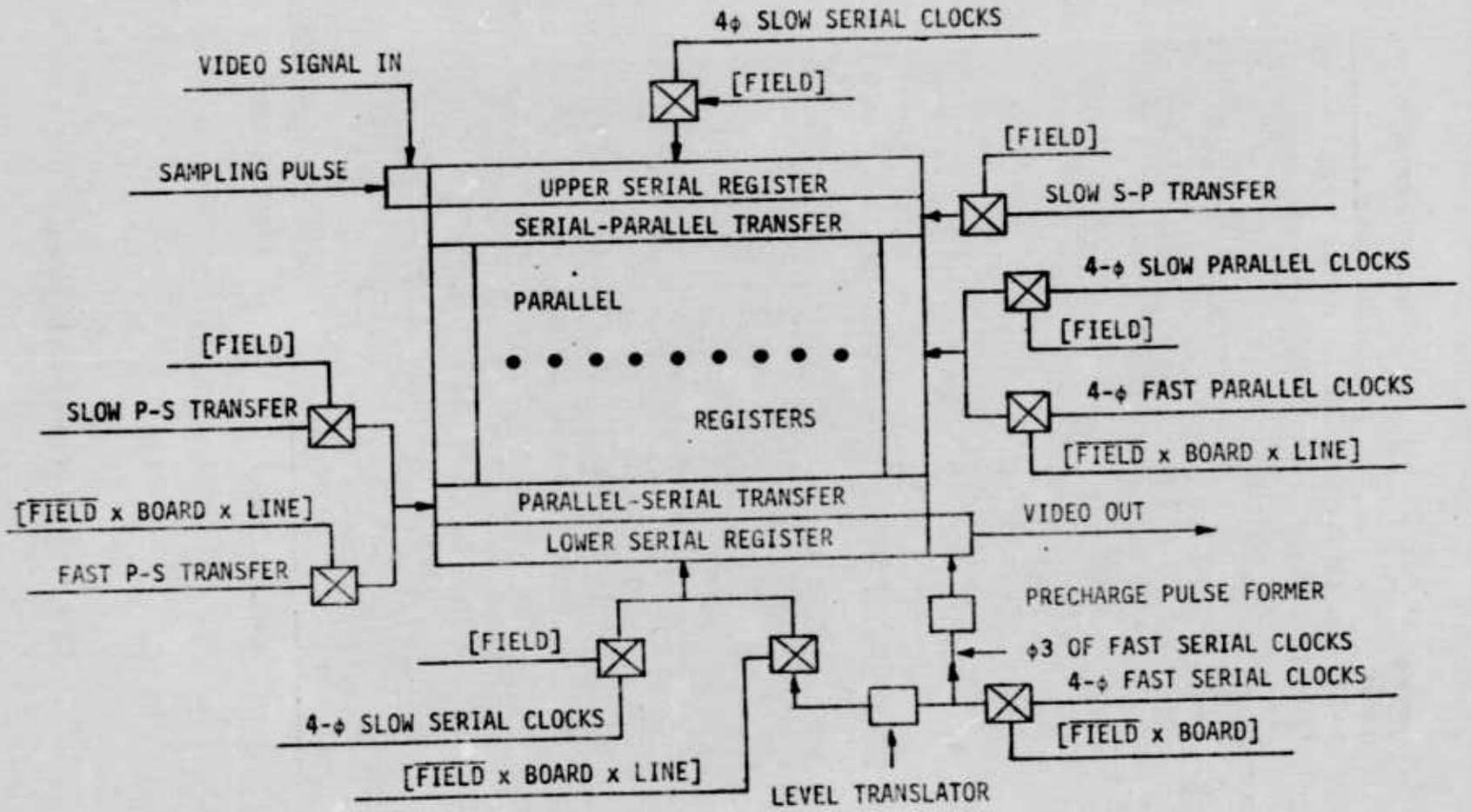

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Figure 12. Schematic of Control Lines and Their Functions for the SPS Array

parallel register, the packets are transferred to the corresponding storage cells of the lower serial register by the action of the slow parallel-to-serial transfer pulse. If the dark-current packets were allowed to pile up in these storage cells, the overflowing charge would "bloom" back upward and fill the storage cells containing signal information. For this reason, the dark-current packets are clocked out of the lower serial register to the output diode by the same 4-phase slow serial clocks that are clocking the signal charge packets into the upper serial register. Note that the slow clocks and transfer pulse trains are all turned on by the same logical conditions that turn on the slow serial clocks; similarly they are ANDed with the [field[logic line.

During the readout phase of bank B, each CCD in the bank is made to read out in turn. When each CCD has its turn to read out, its [board[and [line[logic lines go high. Two logical AND functions are formed, [field × board] and [field × board × line[. Here [board] and [line] represent the high state for the "select" lines for this particular CCD.

As the CCD data are written out, the rows of charge packets in the parallel register are shifted downward one row at a time by the action of the 4-phase parallel fast clocks. As each row reaches the bottom line of this register, the fast parallel-to-serial transfer pulse acts to shift the row into the lower serial register. There each row of packets is then shifted out horizontally to the output diode by means of the fast 4-phase serial clocks. The signal information contained in each individual charge packet is converted from a quantity of charge to a voltage-level shift by the action of the precharge pulse that presets the potential on the output diode node to a reference value just before each charge packet is swept out to the node.

The fast clocks and the fast transfer pulse train are turned on by a logic level that is high only when the horizontal blanking is off and a special viewing "window" for the display is open. In addition, the fast parallel clocks and the fast transfer pulse train are ANDed with the [$\overline{\text{field}}$ × board × line] logic level before being applied to the CCD. The fast serial clocks are generated at TTL level on the central control board and are gated onto the memory boards under the control of the [$\overline{\text{field}}$ × board] logic level. At this point, the level translater (LT) stages raise the voltage level of the clocks to CMOS level; they are gated at this level to the individual CCDs when the [$\overline{\text{field}}$ × board × line[logic line goes high.

The precharge pulse train is generated by taking the falling edges of the Phase 3 fast serial clock waveform, getting this signal onto the memory board under the control of the [$\overline{\text{field}}$ × board] logic level, then using it to trigger the precharge pulse shaper and driver circuit. The output of this circuit is a train of precharge pulses sent to all the CCDs on the board as long as [field × board] is high.

The process by which the precharge pulses along with the Phase 4 clocks cause the stored charge packets to be read out to the output circuit has already been described.

For each of the four separate transfer pulse trains, the timing for the pulses is taken from the related clock waveform; appropriate clockpulse counters are used to determine the required delay between successive pulses.

3. DLM Array

The current form of the concepts for the demultiplex-linear-multiplex (DLM) array and its associated control lines and functions is indicated in Figure 13. A photomicrograph of a test DLM array along with the other test structures and output circuit elements is shown in

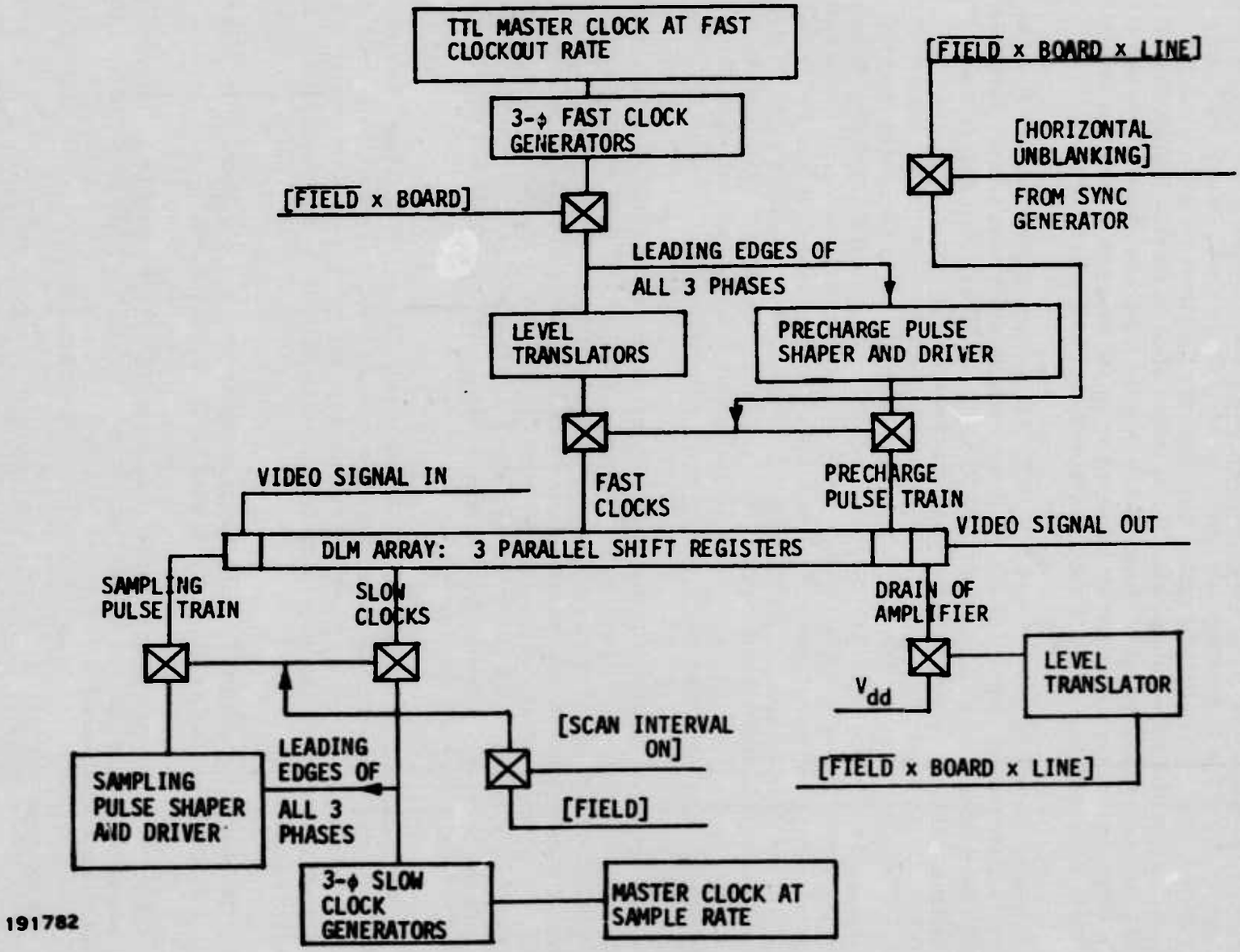

Figure 13. Schematic of Control Lines and Devices for DLM Array

Figure 14. In many respects the anticipated mode of operation of this array is the same as for the SPS array; here we shall deal mainly with the differences and the special considerations.

In the current design configuration the DLM array itself consists of a set of three linear CCD shift registers arranged in parallel so that they can be driven by a single set of three-phased clock waveforms. The inputs to these registers are arranged so that the successive charge packets injected by the sampling pulses are steered first to the first register, then to the second and the third registers. Similarly, the output circuitry is arranged so that successive precharge pulses, working with the single set of fast clocks, cause charge packets first from the first, then the second and third registers to be output to the output node.

At the input end, the master slow clock operates at the signal sample rate. The three clock generators count down from this rate to form the three phases of the slow clock waveform. The

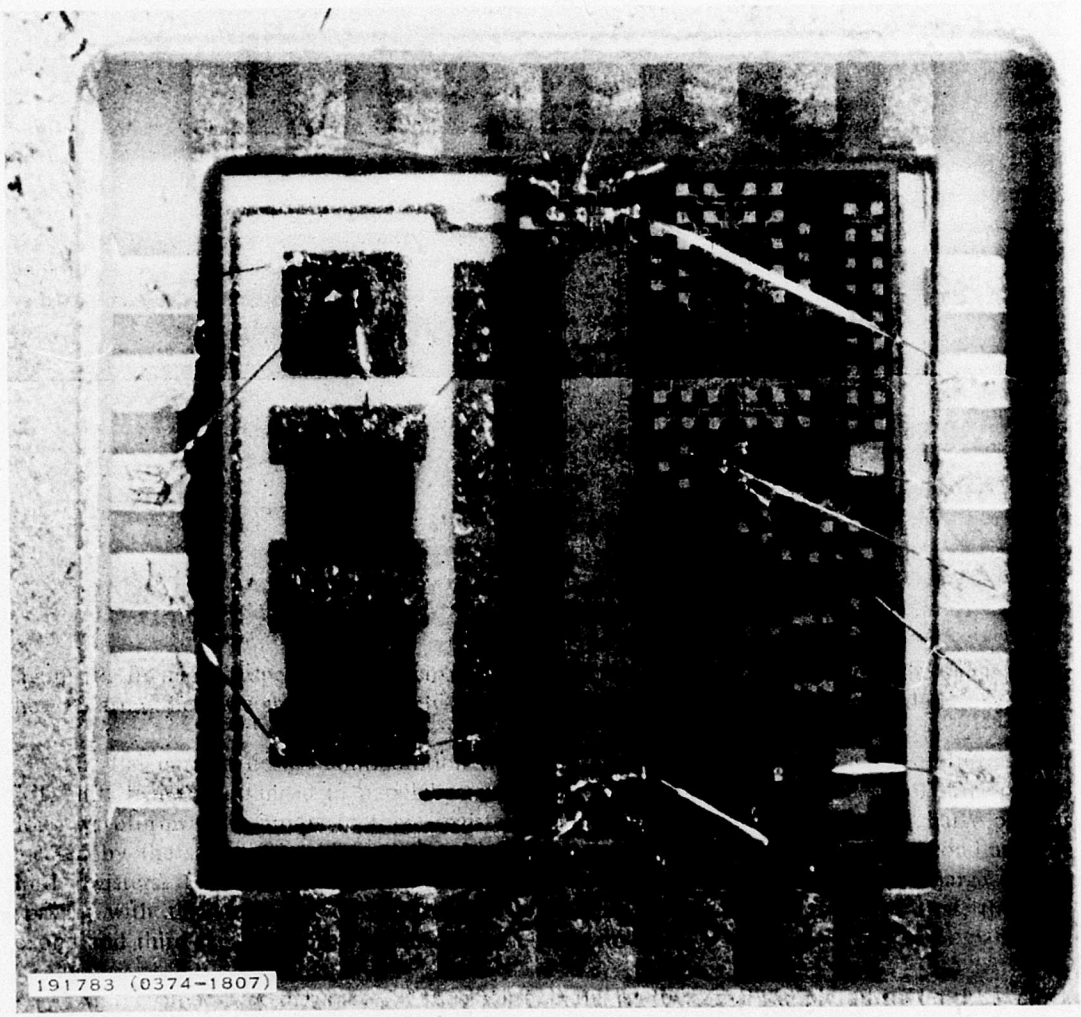

Figure 14. Photomicrograph of DLM Type CCD

sampling pulse train is formed from the leading edges of all the three phases of the three-phase slow clock, instead of from just one of the phases. This is because a sample is formed and a charge packet is injected into each of the registers in turn when the appropriate clock phase is high.

The control of the interval for read-in to the CCD is the same as for the SPS array. The same low-noise input technique will also be used here.

The configuration at the output end is much the same as for the lower serial register of the SPS. The three clock generators count down from the master fast clock, and the precharge pulse shaper triggers on the rising edges of all three phases in order to generate the precharge pulses needed by each of the three registers in turn. The fast clocks and the precharge pulses are gated to the CCD under the control of the [horizontal unblanking] logic line; the gate is preactivated by the [field X board X line] logic level. The circuitry for the output amplifier stages is expected to be the same as on the SPS configuration.

The DLM array is different from the SPS array mainly in the absence of the additional two clock waveforms associated with the loading and dumping of the parallel registers, and also in the absence of the timing requirements for the serial-parallel and parallel-serial transfer pulses. It is anticipated, however, that the DLM array will have a compensating design difficulty arising from the speed and precision required in the process of stopping the read-in and starting the readout. In the SPS array, the lower serial fast clocks can be switched onto the appropriate electrodes and the waveform stabilized before the first parallel-to-serial transfer pulse shifts stored charge packets into the lower serial register. In the DLM, however, there is no such buffer: the fast clocks must be switched on smoothly and very quickly, in a time considerably less than the clockout period. This is necessary in order to keep from impairing any of the stored charge packets.

B. INTERCOMPARISON OF ELECTRO-OPTIC MULTIPLEXER AND CCD IMAGE BUFFER

1. Performance and Operating Characteristics

Performance and operating characteristics of FLIR imaging systems employing DLM and SPS-type CCD buffers are compared in Table 3. The subscripts IB and EO refer to image buffered and electro-optic multiplexed FLIRs, respectively. Both buffers are compared with the electro-optic multiplexer from the modular FLIR. Numerical values given in the table are only approximate since a number of assumptions had to be made regarding image buffered FLIRs. Also, characteristics of standard modular FLIRs will depend upon mission requirements which control specifications of the aspect ratio and the number of detectors. Some of the values in the table are given to three significant figures only for the purpose of indicating that differences are slight; one system will probably be only a little better or worse than the other.

All comparisons are based on a TV-compatible 360-line image with a 4:3 aspect ratio; thus, there are 480 resolution elements in the horizontal scan direction. Systems requiring fewer lines or lower aspect ratios allow for greater performance improvement in the image buffered systems than in the electro-optics multiplexer. This is primarily due to the increased number of samples per resolution element that can be obtained with a given CCD buffer size. Impulse correlation width and edge response are related to the MTF curve. Derivation of the relationships is given in the Appendix. Calculated MTF curves for an image-buffered FLIR are shown in

TABLE 3. PERFORMANCE COMPARISONS FOR CCD BUFFERS

		DLM (0.99995 at 7 MHz)			DLM (0.9999)	SPS (0.9999 at 15 MHz)	
Number of samples per resolution element	N_R	2.25	2.00	1.80	2.25	2.00	1.875
Number of storage cells	N_S	1080	960	864	1080	960	900
Fixed pattern noise frequency ratio	f_L/f_o						
Module 3 (filterable)		1.50	1.33	1.20	1.50	—	—
P-S transfer		—	—	—	—	0.13 and 0.53	0.125 and 0.50
Video sample readout frequency	f_M [MHz]	20.5	18.2	16.4	20.5	18.2	17.0
Clock frequency	f_C [MHz]	6.8	6.1	5.4	6.8	18.2	17.0
Impulse correlation width ratio							
Horizontal	$R_H(1B)/R_H$ (EO)	0.97	0.96	0.96	1.15	0.92	0.92
Vertical	$R_V(1B)/R_V$ (EO)	0.66	0.66	0.66	0.66	0.66	0.66
Edge response ratio	M(1B)/M (EO)	0.99	0.99	1.00	0.96	1.08	1.08
Increase in noise amplitude due to aliasing	$\frac{NOISE_{1B}(f_o)}{NOISE_{EO}(f_o)}$	1.026	1.046	1.072	1.026	1.046	1.060
$\frac{MRT_{H/1B}(f_o)}{MRT_{H/EO}(f_o)}$	2 RC antialiasing filter: $F(1/2) = 0.98\ F_o$	0.93	0.94	0.97	1.01	0.87	0.88
Critical phasing		3 phase clocks at ≅7 MHz Precharge at ≅20 MHz				4 phase clocks at ≅18 MHz Precharge at ≅18 MHz P-S transfer, parallel phase 4, serial phase 2.	

Figures 15 and 16 together with the MTF curves of an E-O multiplexed FLIR. The MTF for the E-O multiplexer and for the image buffer alone are shown in Figure 17.

A sampled system will always have some aliased noise folded into the system passband from higher frequencies,unless the sampling rate is very high or unless very sharp filters are utilized; neither of these is practical in a compact low-power image buffer. The strength of the aliased noise at the resolution frequency, given in Table 3, is computed for a double-RD antialiasing filter with a break frequency chosen to be consistent with realizable circuit parameters. The on-chip filter can probably be improved somewhat by making use of an active component.

Minimum resolvable temperature difference (MRT) is directly related to the aliased noise and inversely related to the MTF of the system:

$$\frac{MRT_{IB}(f_o)}{MRT_{EO}(f_o)} = \frac{NOISE_{IB}(f_o)}{NOISE_{EO}(f_o)} \times \frac{MTF_{EO}(f_o)}{MTF_{IB}(f_o)}$$

The table and the MTF curves show there is relatively little difference between the image buffer systems and the modular FLIR E-O multiplexer with regard to horizontal impulse correlation width, edge response and MRT. This is because the present modular FLIR performance in these categories is not significantly degraded by the electro-optic multiplexer; the same should be true for the CCD image buffers.

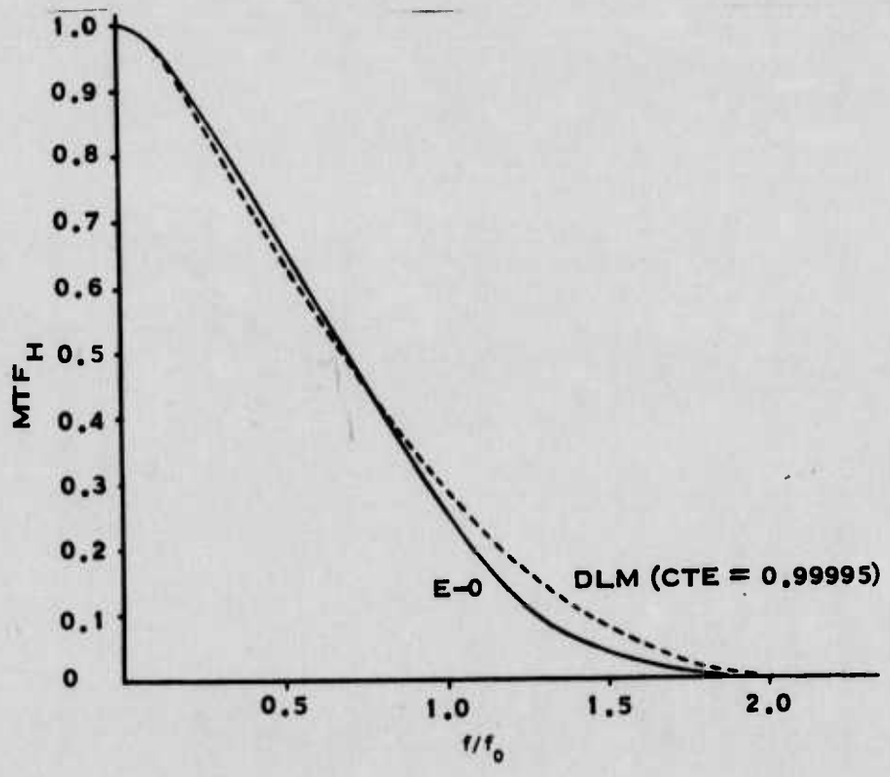

Figure 15. Total System MTF in Horizontal Direction

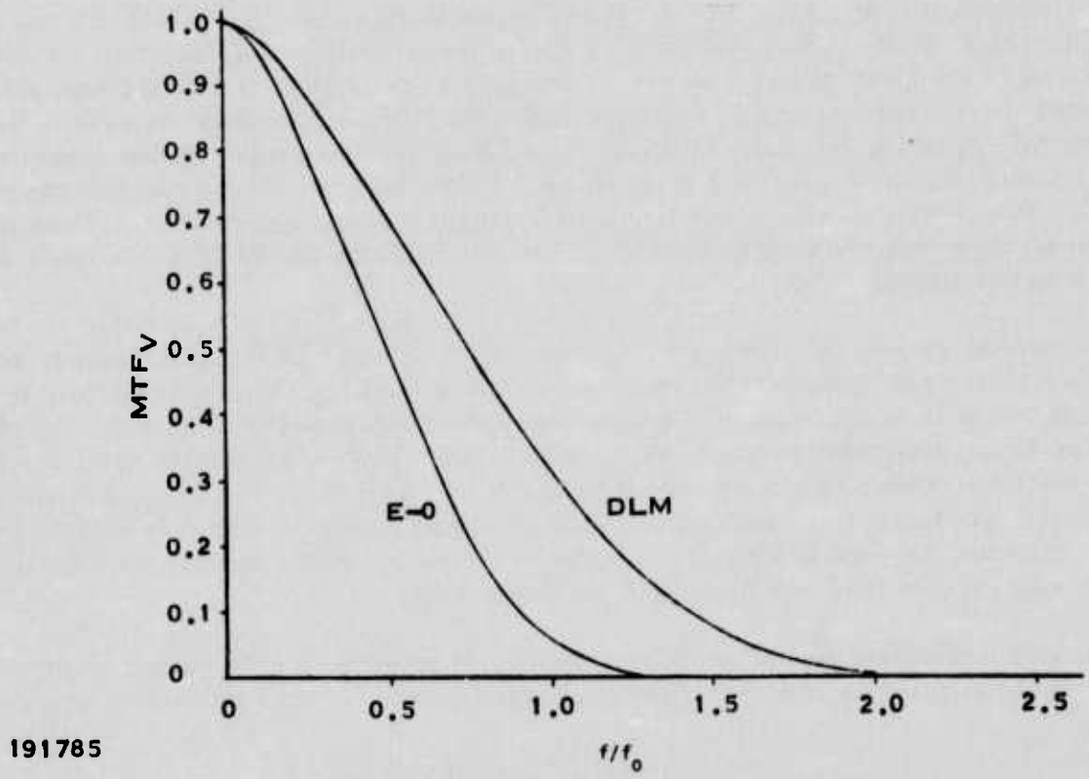

Figure 16. Total System MTF in Vertical Direction

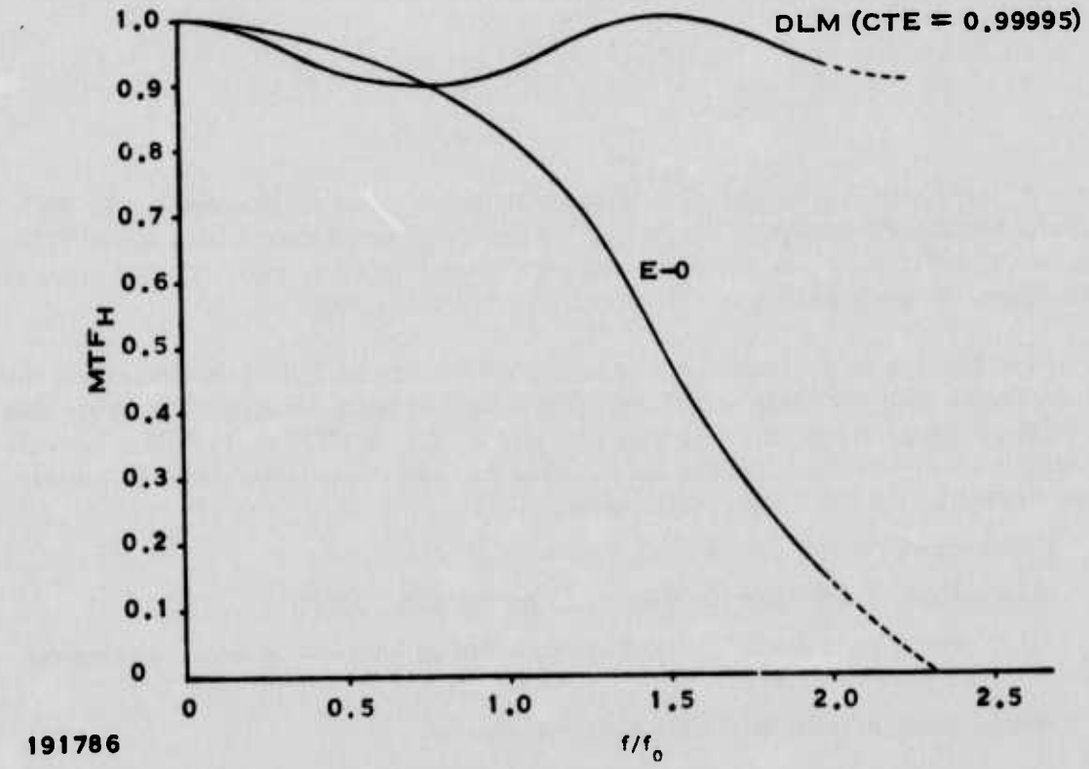

Figure 17. Component MTFs in Horizontal Direction for E-O Multiplexer and for DLM Image Buffer

The 50 percent improvement that image buffers are to provide in vertical MTF is a direct result of the shape of the LEDs currently being used in the E-O multiplexer. Each LED is made twice as long as its corresponding detector, to eliminate noise patterns that would otherwise appear when the TV raster is used to image the LED raster. This problem does not occur in the image-buffered systems because each TV line is formed from its corresponding IR line. However, the main reasons for developing CCD image-buffered FLIRs are improved size, weight, power, and cost, rather than the prospect of significantly improved image quality. One purpose of Table 3 is to show that the imagery from image-buffered FLIRs should be at least as good as imagery from electro-optic FLIRs.

The second purpose of Table 3 is to show the effects of particular parameters on performance of the two types of CCD image buffer. Both must be TV-compatible; thus, the output data rate is to be the number of storage cells divided by the active horizontal TV scan time, 53 μs. Since CMOS devices cannot now be made to operate well at frequencies much above 20 MHz, the total number of storage cells is limited to about 1000. On the other hand, if all data from the detectors is to be used, there should be at least as many storage cells as there are resolution elements; for good imagery there should be at least 50 percent more. In addition, the higher the sampling rate, the lower the level of the aliased noise.

The effect of aliasing on the overall system S/N was estimated for the current model of the noise spectrum at the sampling point. The results for 2.25 samples per resolution element are as follows:

Relative Frequency (F/F_0)	Reduction in Overall S/N due to Noise Foldback
0+	0.01
0.5	0.03
1.0	0.06
1.5	0.14

There is one other bound on the sampling frequency. For frequencies up to about 10 MHz, charge-transfer efficiencies (CTE) of 0.99995 can be obtained using buried-channel CCD techniques. At higher frequencies the CTE per stage begins to fall rapidly, so that even at 15 MHz the highest presently achievable CTE appears to be about 0.9999.

The effect this has on performance parameters can be seen in Table 1 by comparing the two DLM memories with the same 2.25:1 sampling ratio and with different CTEs. Note that since the DLM clocking rate is only one-third the readout rate, a CTE of 0.99995 is possible with a 20-MHz readout rate. In summary, the sampling rate and the resulting number of storage locations are limited by the following considerations:

CMOS input, output, and clocking should be 20 MHz or less.

Achievable CTE decreases for clock rates greater than 10 MHz.

There should be at least 1.5 times as many storage locations as resolution elements, for good imagery.

Aliased noise increases as the sampling rate decreases.

The DLM buffer is recommended in preference to the SPS buffer for two main reasons: it requires less complex driving circuitry, and fixed pattern noise arising from slight imperfections in the DLM buffer occurs at higher frequencies than for an SPS buffer and can therefore be more easily eliminated. These two factors are of such importance that they outweigh the slightly better performance of the SPS buffer in impulse correlation area, edge response, and MRT.

2. Drive Circuitry

For both buffers, the output circuit requires precisely-timed precharge pulses at readout rates of about 20 MHz. The DLM is driven by only three clock lines, which operate together alternately at the input and the output frequency. The SPS, on the other hand, has four clock lines that operate at the serial-in rate, four clock lines that operate alternately at the parallel-in and the parallel-out frequencies, and four clock lines that operate alternately at the serial-out and the serial-in frequencies. The relative phases in each set of clock waveforms must be precisely controlled; in addition, serial-parallel transfer-gate pulses and parallel-serial transfer-gate pulses must be precisely timed with respect to the serial and parallel clock waveforms. One of the most serious difficulties for the SPS array in this regard is that its serial-out register has to be clocked out at the charge packet output rate; for the DLM array, the highest clocking frequency is only one-third the output rate.

In the application of CCD image buffers to FLIR systems, it is essential that the image buffers be able to read out backwards as well as forward, in order that the return swing of the scan mirror can be used and the scan efficiency kept appropriately high. For the DLM array, all that is needed for the appropriate CCDs to read out backward is for two of the phases of the fast clock waveform to be connected in reverse to the CCD clock inputs. Note that the connections to the precharge do not need to be switched, because the precharge is used only with the fast clocks. In the SPS buffer, on the other hand, the task of adapting to two-way scan is markedly more complex. Not only do Phase 2 and Phase 4 have to be reversed for both the fast-serial and the fast-parallel clock waveforms; in addition, the source line for controlling the serial-to-parallel transfer gates needs to be shifted from a logic network driven by the slow serial-in clock waveforms to a different logic network driven by the fast serial-out clock waveforms. This is because there has to be a transfer across the interface between the parallel register and the upper serial register both during the read-in and the readout processes.

Thus, for the SPS buffer, there are more clock waveforms, more logic networks for generating timing pulses, and more clock lines to be connected and switched. The additional complexity is even greater for those CCDs that are to be read out backward. The additional connections and circuitry that are required and that have to be in the CCD package itself mean that each SPS memory element will necessarily occupy more space, so the SPS buffer cannot have as high a packing density as an equivalent DLM buffer.

Consideration was given to placing the CCD drivers on the same chip with the memory array in order to further reduce the size and power consumption of the image buffer. This has been rejected at the present time because of possible degradation of CCD dark-current characteristics when both CCD and MOS devices are fabricated in the same process run.

Since device development was not a part of the contract, integration of these structures on the same chip will be the subject of future development proposals.

3. Fixed Pattern Noise

For the two types of buffers, the fixed-pattern noise arises from different main sources and shows different characteristic frequencies. For the DLM buffer, the main sources are variations in the capacitances of the first electrodes of the three channels in the DLM, and also variations in the threshold voltage for these electrodes. The characteristic frequency of the resulting noise is effectively at $f_s/3$, where f_s is the sampling frequency. If f_s is 2.25 times the resolution-element frequency, and if this is twice the maximum frequency f_0 of the video-signal passband, then a signal at $f_s/3$ is at $1.5\,f_0$. A relatively low-level signal at this high a frequency can almost assuredly be notch-filtered out of the output video signal with only minimal impact on the system MTF.

For the SPS buffer, on the other hand, the fixed-pattern noise arises mainly from the fast parallel-to-serial transfer pulse and the fast parallel clocks. Its characteristic frequencies are $f_s/30$ and $4f_s/30$. If f_s is twice the resolution-element frequency and thus four times f_0, then these frequencies become $0.13\,f_0$ and $0.53\,f_0$. Any attempt to notch-filter these frequencies out from the video output would have a marked effect on the system MTF. As was noted earlier, the output clock frequencies for the SPS are already, at 2 X resolution frequencies, pushing the limit of CCD and CMOS technology, so there is little prospect of being able to raise the fixed-pattern noise frequencies appreciably, to make filtering easier.

C. OPTIMUM MEMORY ELEMENT

The DLM CCD configuration has been selected as optimum for the image-buffer application. At least one thousand storage locations are needed for adequate sampling of a FLIR image line. Charge-transfer inefficiency would cause unacceptable MTF loss in a linear array even with a CTE = 0.99995. Since the clock rate for a linear array would have to be above 20 MHz, achievable CTEs are not as high as for the DLM. Therefore, even though the linear array can be operated with the simplest clock scheme and input circuitry, the high clocking frequency and array length required make it less attractive than SPS or DLM geometries.

The DLM is favored over the SPS array on the basis of reduced complexity and the frequency of the primary fixed pattern noise as discussed earlier. In summary, SPS requires four clock frequencies plus precisely timed transfer pulses, while DLM clocking is as simple as for a linear array and is one third the frequency. Both SPS and DLM have fixed pattern noise arising from distribution of the signals over different paths through the CCD. However, in the DLM array the fixed pattern noise is at a frequency higher than the resolution frequency, while for an SPS array it appears in the pass band.

The 1080 stage length has been chosen as an optimum size with present technology. It is important to sample at as high a rate as possible to reduce the effect of aliasing. The upper limit is imposed by the speed with which the MOS output circuits must process the data for TV display. The 1080 stage length represents 2.25 samples per resolution element for a modular FLIR with an output rate of about 21 MHz. This is as fast as the output circuits can be operated reliably.

SECTION IV
MEMORY ELEMENT LAYOUT

A. INPUT STAGE

The study and development of CCD input circuitry has advanced to the point where the choice of technique for the input process is fairly clearly indicated. The chosen technique involves feeding in the input signal on the input gate and performing the sampling function by pulsing the input diode. This technique appears to be the least noisy way of injecting charge packets into the image buffer. In fact, the associated noise level has been shown to approach quite closely the ideal limiting level. The technique was used with good results in the SPS CCD image buffer breadboard demonstration program.

Figure 18 shows the input configuration for the image buffer and the energy level of the electrons in the potential wells during and just after the sampling pulse. Figure 19 shows the relative timing of the sampling pulse and the clock waveforms. During the negative-going sampling pulse on the input diode, the electron energy at the input rises to the point that electrons from the diode can flow over the variable potential barrier under the input gate and into the fully formed potential well formed by the on-state clock voltage on the input clock phase electrode. This condition continues until the electron energy in the input well is the same as that of the input diode. When the electron energy level at the input diode falls, the excess charge in the input well is drained off along the conduction channel below the input gate until the peak energy level in the input well is the same as under the input gate. The potential on the gate at that instant is just the signal voltage that is to be sampled. The quantity of charge left in the Phase 1 charge packet is proportional to the potential difference between the input gate and the Phase 1 electrode, which is in its on state. Thus, this amount of charge is a measure of the signal amplitude at the end of the sampling pulse.

Note that the effective potentials sensed by the charges at the input stage are biased with respect to the voltages actually applied to the input diode by just the amount of input-diode voltage threshold, which is about 13 volts. Thus, when the applied voltage on the diode is +13 volts, during the sampling pulse, as shown in Figure 19, the energy level of the electrons under the neighboring input and Phase 1 electrode is about zero volts. Thus charge can flow over the positive potential barrier formed at the input gate by the input signal that is biased so as to be always well above ground.

Shortly after the end of the sampling pulse, the Phase 2 clock comes on, causing the charge packet to be shared between the Phase 1 and Phase 2 potential wells and eventually to be transferred entirely to Phase 2.

Note that, in this case, at the end of the sampling pulse, the flow of charge over the input-gate potential barrier is exclusively unidirectional, from the Phase 1 charge packet to the input diode. This is in contrast to the situation in which the roles of the input diode and gate are interchanged; here the charge can flow both ways from the collapsing well under the input gate, and the statistical uncertainty in the direction of movement of individual electrons adds significantly to the total "noise" represented by the charge packet. Thus, the chosen technique described here is a minimum-noise method of injection signal samples.

If the signal voltage on the input gate were to rise in the interval between the end of the sampling pulse and the start of the charge sharing between Phase 1 and Phase 2, additional charge would be lost from the charge packet; in this case, the rise of the Phase 2 clock voltage would become the sampling instant rather than the end of the sampling pulse. Thus there is hysteresis in the sampling process, since the sampling occurs later in the clock cycle for a rising signal voltage than for a falling voltage. This hysteresis produces some distortion of the higher spatial frequencies in the input signal. The amount of distortion is kept small because the time between the end of the diode sampling pulse and formation of the Phase 2 potential well is only a very small fraction of a clock cycle.

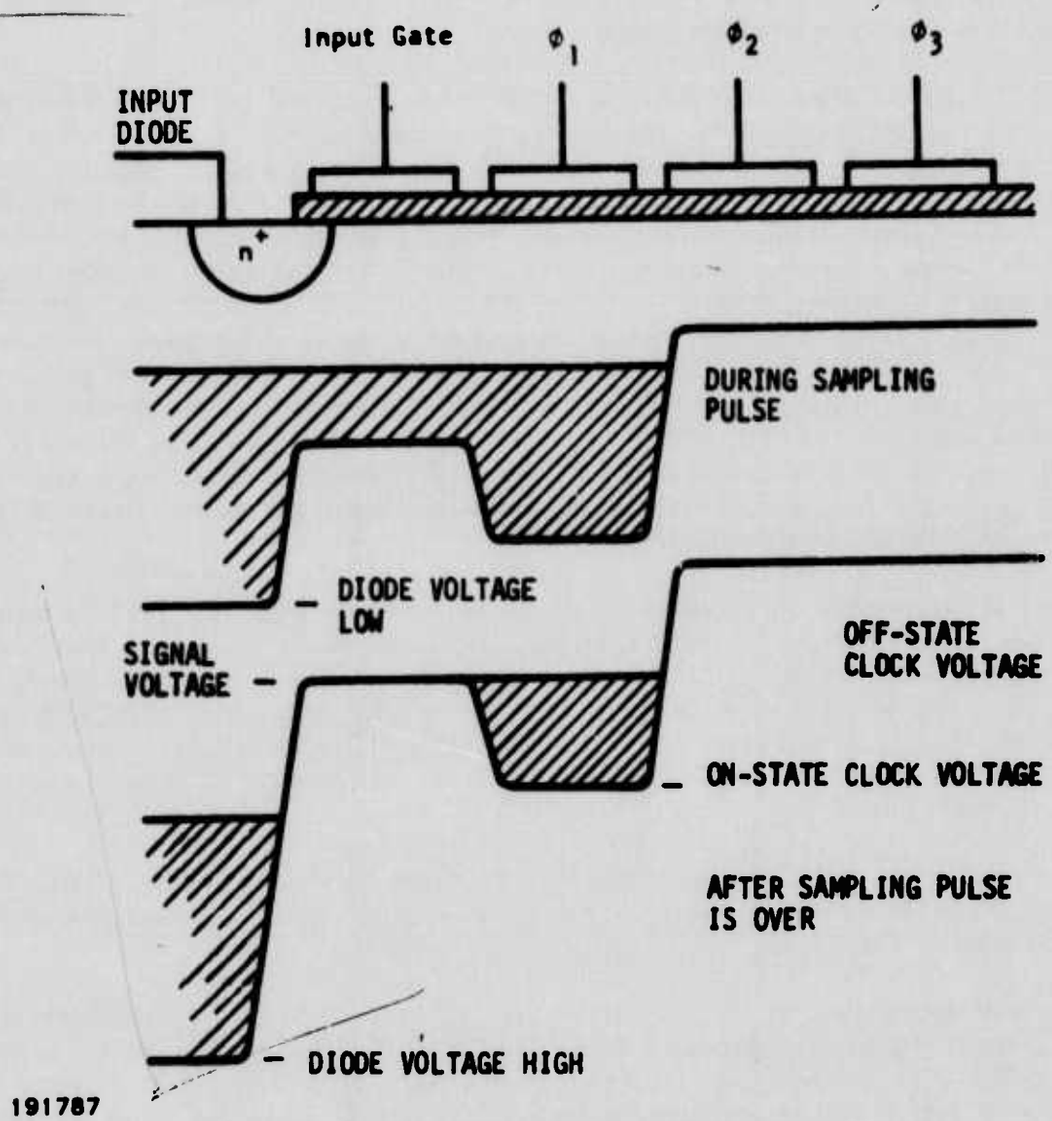

Figure 18. Schematic of CCD Input Configuration and Electron Energy Levels During and After the Sampling Pulse

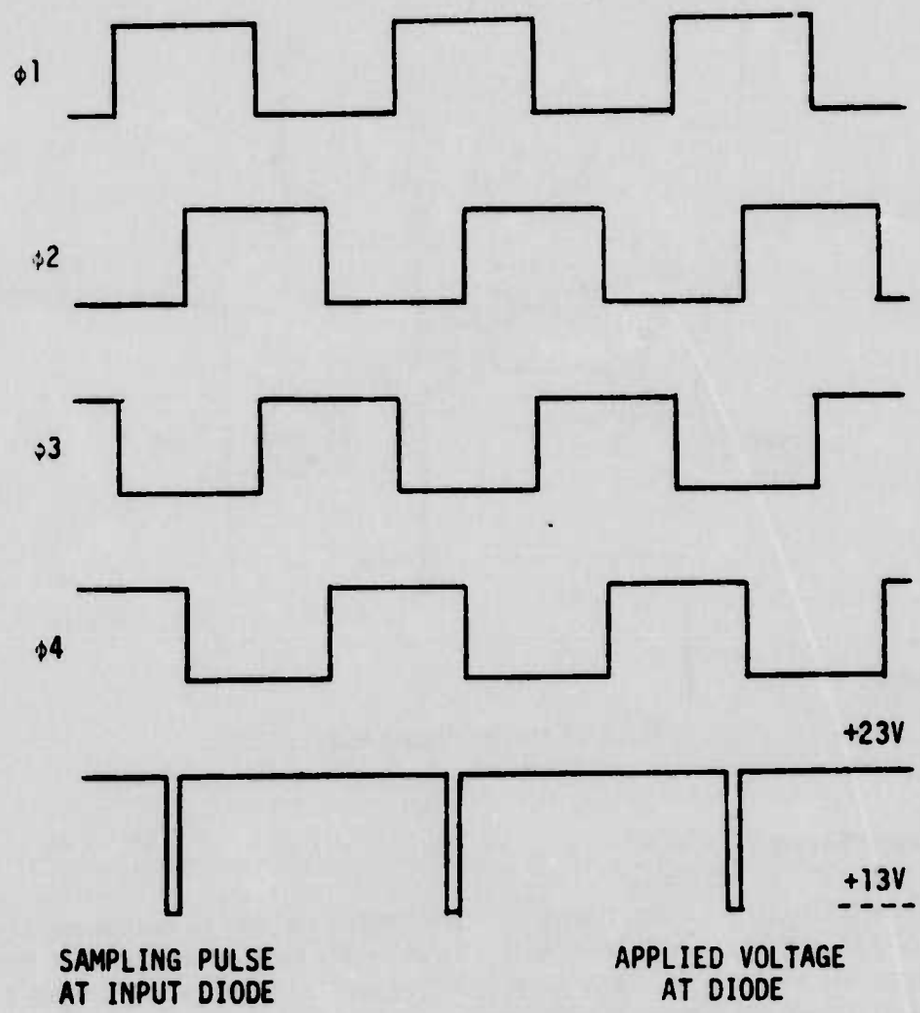

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Figure 19. Upper Serial Slow-Clock Waveforms and Sampling Pulse Train

B. OUTPUT STAGE

The design of a fully adequate output stage is complex and is taking more effort than had been anticipated when work in analog memories first started. The output circuit is the source of dc offsets due to MOSFET threshold variations and other causes. In addition, it is the source of some feedthrough of high-frequency clock pulses, which adds to the system noise, and also of some line-to-line gain variations, which perturb the image display. The output circuit that was used in the SPS breadboard demonstration represents the current state of the art and is what would be proposed for use in this program. It is hoped, however, that a fully differential-type output circuit can be developed before the final decision has to be made about the actual circuit to be used. Such a differential circuit can be expected to suppress most of the dc offsets and feedthroughs, and also most of the time-varying part of the gain variations.

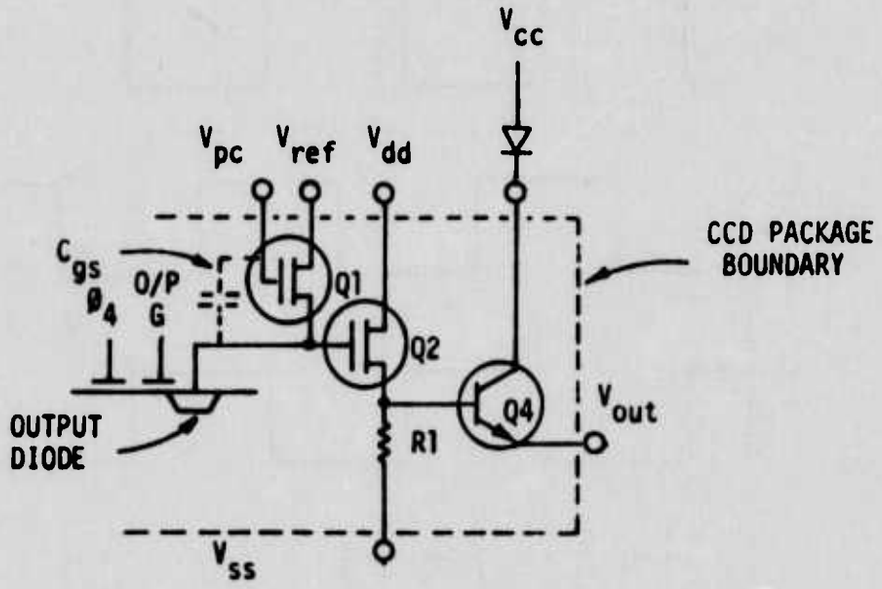

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Figure 20. On-Chip Output Stage of CCD

1. Precharge Theory

The output circuitry consists mainly of a precharge stage and an output amplifier as shown in Figure 20. The precharge stage takes each charge packet that is being output from the CCD and transforms the amount of charge in the packet into a corresponding output voltage level, which it holds during the output hold interval. It then resets the output circuit to a reference state, so that the output voltage level for each charge packet depends only on the amount of charge in that particular packet. The output amplifier transforms the output voltage level from a very high-impedance source to a low-impedance source, so that the stray capacitances in the output circuit do not limit the high-frequency capability of the CCD.

The oscilloscope trace shown in Figure 21 is a typical CCD output waveform. This is shown schematically in Figure 22, along with corresponding waveforms of the precharge pulse and the clock pulse for the last CCD storage electrode Phase 4.

The output node consists of the anode of the output diode, plus the source side of Q1 and the gate of Q2. The precharge pulse on the gate of Q1 causes the output node to be charged to a voltage that is determined by the voltage V_{pc} of the precharge pulse and the threshold voltage V_T of Q1. For high-speed operation, V_{pc} is typically a few volts higher than the Q1 drain supply voltage V_{ref}. Q1 can be considered as a common-drain stage charging the output-node capacitance C_{node} connected to its source. The source current is given by

$$i_s = g_m (V_{GS} - V_T)$$

Figure 21. CCD Output Waveform, Including Precharge Pulses

where V_{GS} is the gate-to-source voltage. If $V_{GS} - V_T$ is greater than the drain-to-source voltage V_{DS}, then g_m depends on V_{GS}. As C_{node} charges up toward $V_{pc} - V_T$, V_{GS} decreases, so g_m decreases, and the charging current falls off more rapidly than if g_m were constant.

When the voltage of C_{node} reaches V_{ref}, V_{DS} goes to zero, Q1 turns off and V_{node} is clamped at V_{ref}. The voltage on the gate-to-source capacitance C_{gs} for Q1 is then fixed at $V_{pc} - V_{ref}$. At the end of the precharge pulse, the gate of Q1 is effectively grounded, so the charge q_{gs} bound on C_{gs} is released, decreasing the charge on the output node and increasing its effective capacitance. Thus when the precharge pulse falls, V_{node} falls by

$$\Delta V_1 = V_{pc}\, C_{gs}/(C_{node} + C_{gs})$$

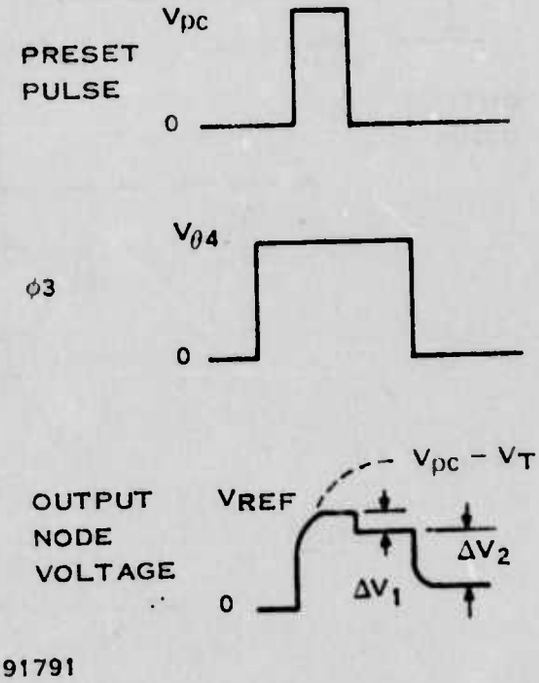

Figure 22. Clocking, Precharge and Output Waveforms

When the clock voltage V (Phase 4) on the last CCD storage electrode falls, shortly after the precharge turnoff, the charge packet q (packet) stored in the well formed by that electrode is swept over the low potential barrier (about 2 volts) under the output gate electrode and onto the output diode. The addition of this negative charge further decreases V_{node} by the amount

$$\Delta V_2 = q\ (\text{packet})/(C_{node} + C_{gs})$$

Here ΔV_2 is the signal information amplitude. These three successive values for V_{node} are shown in the output-node waveform in Figure 22. At this point the clocked-out charge packet has been transformed to a voltage excursion at the output node.

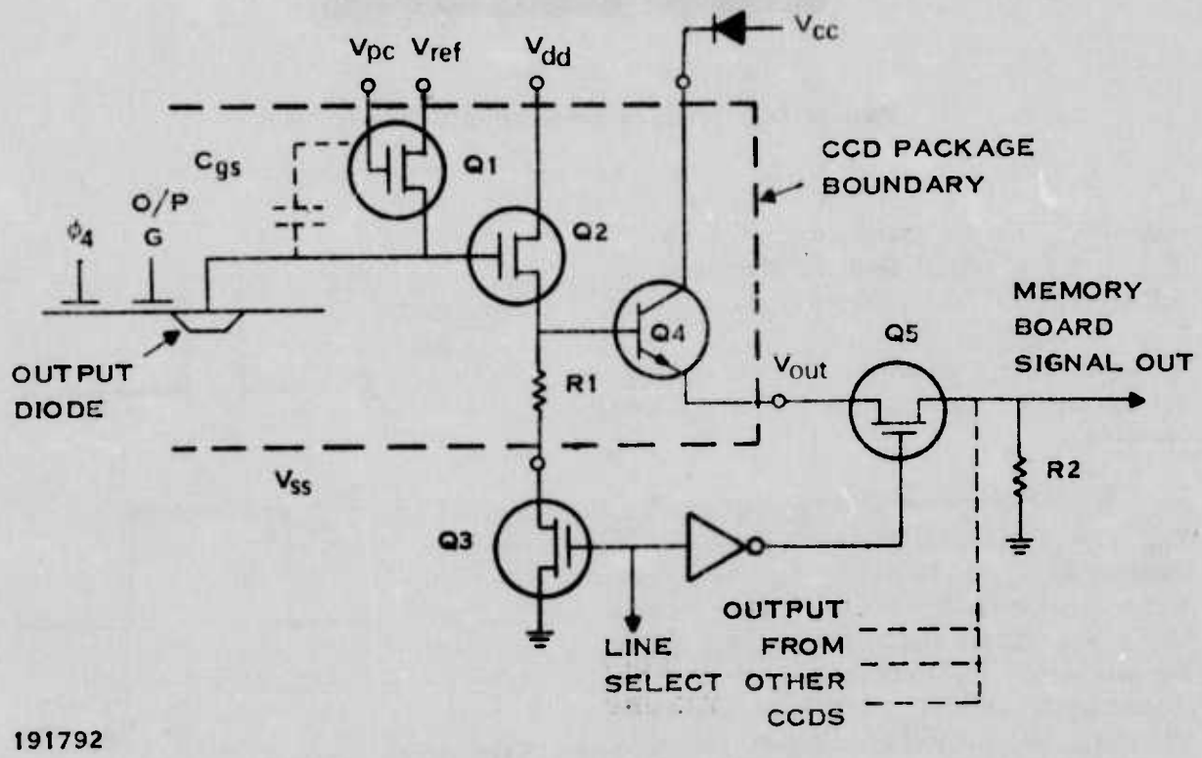

Figure 23. Output Stage of CCD for SPS Array

2. Load Switching

The source follower Q2 converts the impedance level of ΔV_{node} from a very high level, corresponding to C_{node} being very small, to a relatively low level. If the source follower were on all the time, the heat it would dissipate would degrade the operation of its associated CCD by raising its dark current. For this reason, a line-select MOSFET switch Q3 is added, as shown in Figure 23, so the source resistor R_1 is returned to ground through the relatively low on-resistance of Q3 only when that particular CCD is clocking out its line of video information.

Output from the source of Q3 is further reduced in impedance level by the emitter-follower Q4. Both R_1 and Q4 are contained as separate chips within the multi-chip

package along with the CCD. Only with Q4 included in the package could the impedance level of the signal level be made low enough that the effect of pin out and other stray capacitance at the package output point would not degrade the required high-frequency performance of the system.

The same line-select pulse that returns R_1 to ground serves to connect the emitter output of Q4 to its resistor R_2 through the series switch Q5. The on-resistance of Q5 is kept small with respect to R_2, to keep down the signal loss in Q5. The value of R_2 and the on-resistance of Q5 are chosen to give the optimum value of collector current for Q4, to give the lowest output impedance. Note that all the CCDs on a memory board use a single common resistor R_2, since only one of the CCDs at a time will be switched onto it via the line-select system.

3. Stage Switching

The output stage used in the SPS breadboard demonstration has been described. A differential-type output circuit was mentioned as a possible replacement. Figure 24 is a schematic of a fully differential-type output circuit. This circuit has not been built and no tests have been made to determine its effectiveness in suppressing dc offsets and feedthrough noise.

The operation of this circuit is similar in principle to the output circuit just described, in that a precharge stage takes each charge packet that is being output from the CCD and transforms the amount of charge in the packet into a corresponding output voltage level. Between readout of each cell, the output circuit is reset to a reference state, so that the output voltage level for each packet depends only on the amount of charge in that packet. An emitter follower amplifier transforms the output voltage level from a very high impedance source to a low-impedance source.

There are three principal differences between the circuit of Figure 24 and the earlier version. First, this is a differential circuit. One-half of the output stage converts each charge packet shifted out of the CCD buffer to a signal voltage while the other half does the same for the charge shifted out of a dummy CCD array consisting of only a few cells. The reference voltage from the dummy array is to be subtracted from the signal voltage after the emitter follower amplifier.

The second difference is that the line select switch to turn on the output circuit has been placed in the drain line of the source followers Q2 and Q3 instead of the source side in order to eliminate switch noise from the signal.

The third change is the substitution of active loads Q6 and Q6′ for resistive loads, thereby allowing placement of the source follower load on the CCD chip instead of separately within the hybrid package.

C. SCAN AND CCD CHIP

One of the important topics considered in this study was the comparison of the SPS and the DLM arrays in their adaptability to a backward as well as a forward readout. The backward or last-in-first-out (LIFO) readout is needed in order to produce a normal TV image field from a FLIR image read-in during a return scan of the scanning mirror. A study has already been made of the prospective complexities of adapting the SPS array to a LIFO capability. The DLM array has also been studied in this regard. Adapting the DLM to meet the LIFO requirement will be

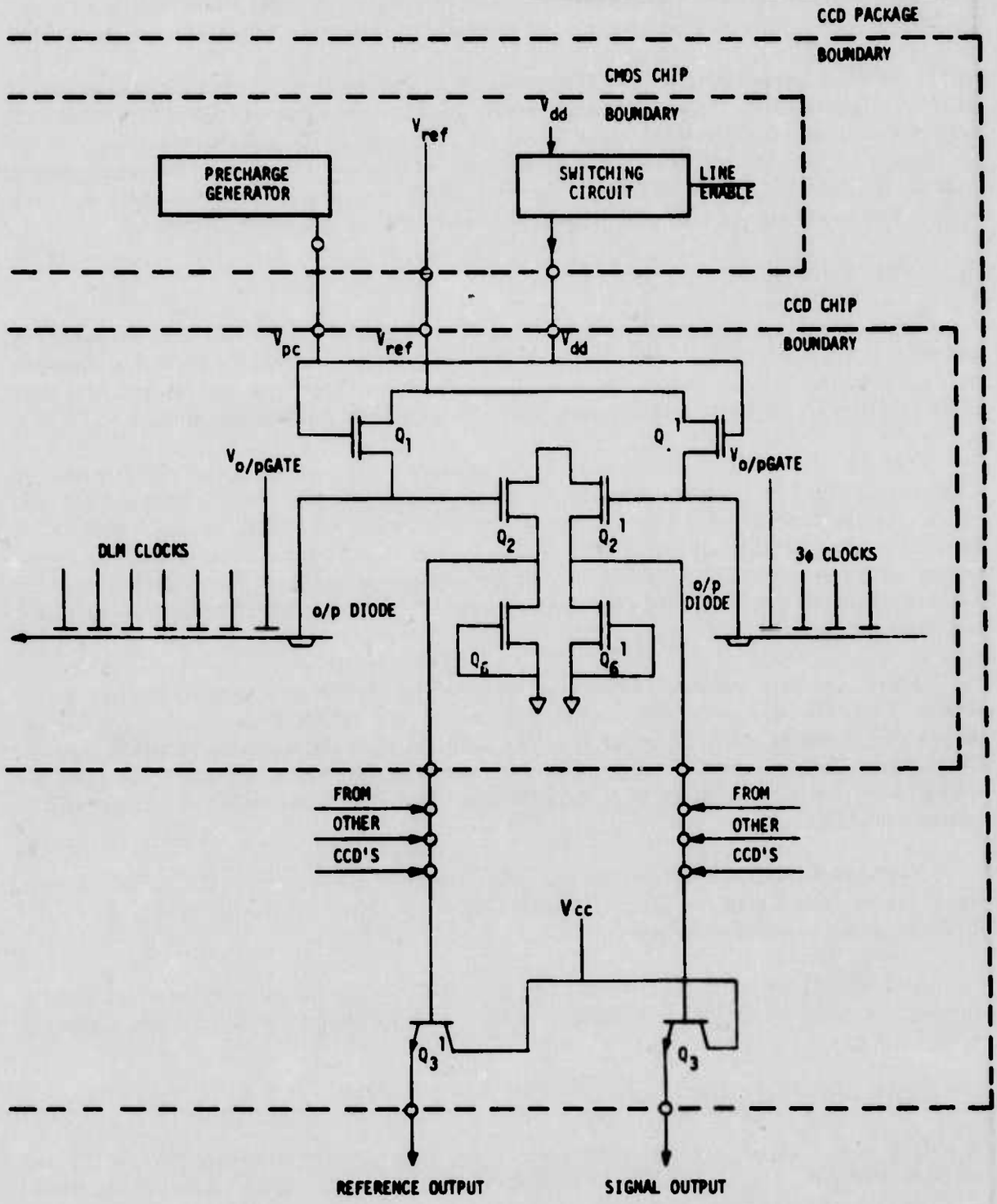

Figure 24. Differential Output with Active Load

significantly simpler than for the SPS, mainly because of the simpler although more exacting clocking arrangements. A conceptual design study has been made to develop candidate switching arrangements by which the connections to the input circuit elements can be adapted to serve as the output circuit elements. The switching will be done under the control of the [field] logic line.

It is expected that any particular CCD will be permanently wired for either LIFO or for normal readout. Thus, memory bank A with all its associated memory boards, for example, will be read into during the forward scan of the FLIR mirror and will provide field B by LIFO-type readout. Thus there will be no need to be able to switch an individual CCD from one form of readout to another.

Figures 25 and 26 show the external connections and the interconnections for the FIFO and for the LIFO CCD chips. The anti-aliasing filter is to be formed on the same substrate; its output is to be connected to the appropriate bond pad of the CCD. In both figures, like-lettered points are to be bonded together. This arrangement allows the same basic CCD chip to be used in both the LIFO and the FIFO modes. Table 4 lists the functions and nominal voltages of the connections to the chip. Note that the output emitter-follower stage is actually on a separate chip and is to be shared by all the CCDs in the package.

TABLE 4. CONNECTIONS AND THEIR FUNCTIONS FOR THE CCD CHIP

Name	Function and Level
FIFO Mode	
Signal in	To input of antialiasing filter; +6 V ± ≅ 2 V
Sampling pulses to input diode	Base level ~ +20 V; pulses to ~ +13 V while input is being sampled
Points B	Filter output connected to input gate
Phases 1, 2, 3	0 to +10 V
Output clamp gate	Logical equivalent to field × board × line
Switched V_{dd}	Connected to V_{dd} during field × board × line
Changes and Additions for LIFO Mode	
LIFO gate	Connects input/output gate to output of antialiasing filter only during loading; otherwise connects it to +2 V
Points B	Filter output/+2 V connected to input/output gate
+20 V	Unused diode, biased to dump clocked-out dark-current during load
Sampling pulses to input diode	Combined function of +15 V for drain control and of input for sampling pulses

Note: All references to field for FIFO become field for LIFO

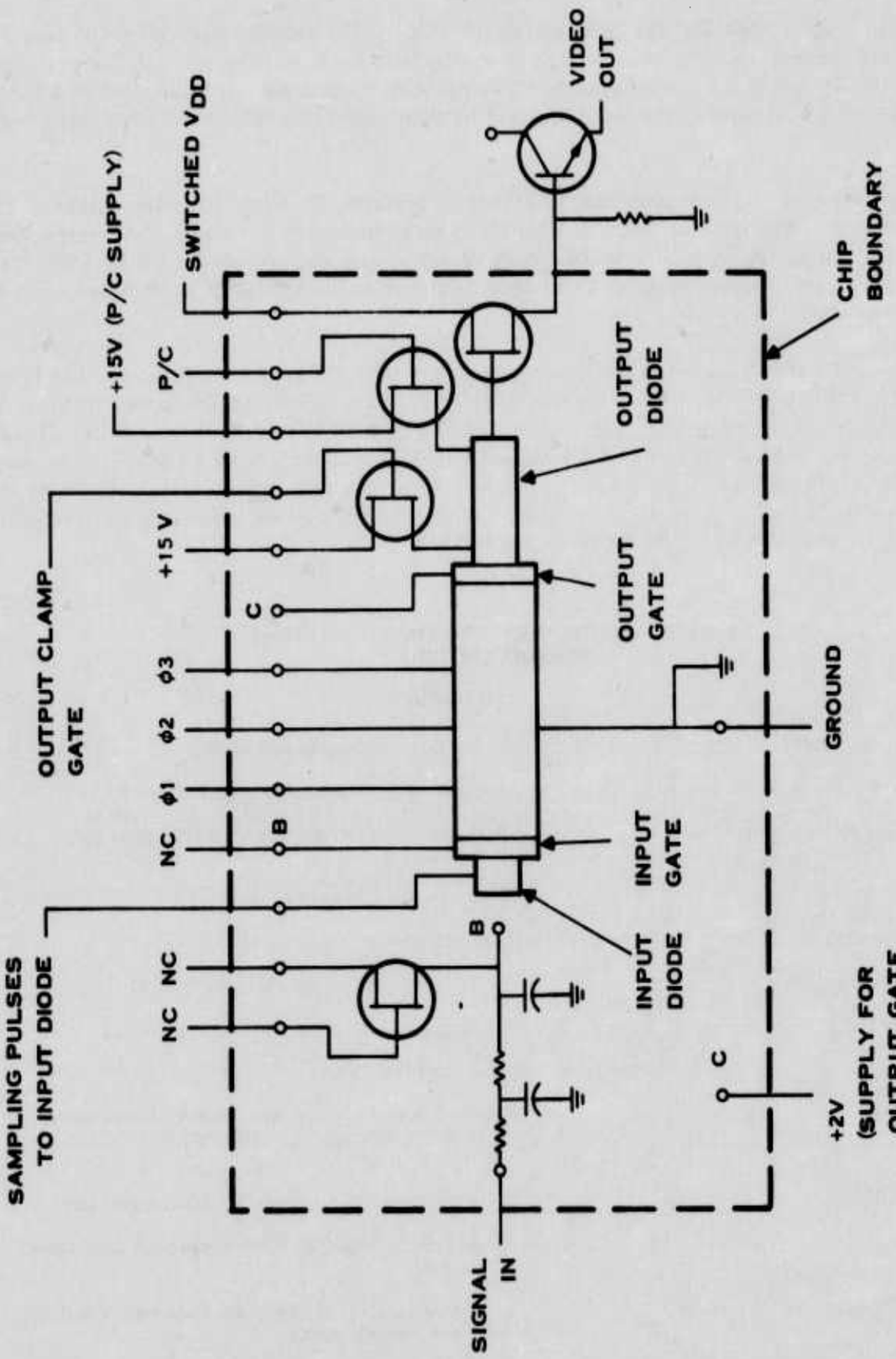

Figure 25. Internal and External Connections for FIFO-Mode CCD Chip

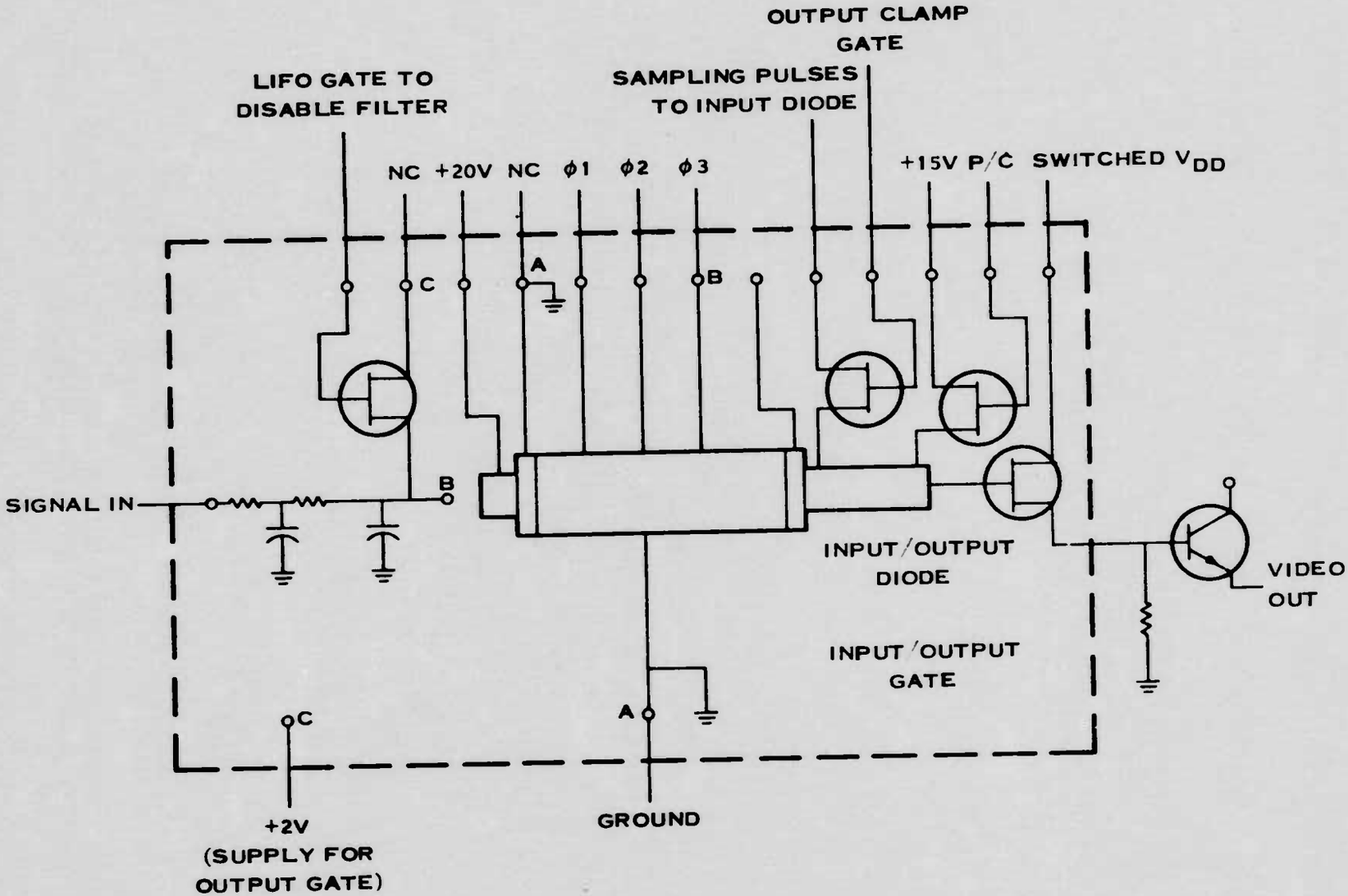

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Figure 26. Internal and External Connections for LIFO-Mode CCD Chip

SECTION V
IMAGE BUFFER ORGANIZATION

A. BASIC CONFIGURATION

1. Functions

The CCD image buffer module is divided into three subunits of control, memory and post-conditioner as shown in Figure 27. The control unit must generate the synchronization signals for the IR scanner and the CRT, the "load" and "dump" clocks, and all of the enable and blanking signals which tell each CCD when to read information in from the parallel video and when to write it out to the CRT. These functions are shown in block diagram form in Figure 28.

The memory itself will be composed of a set of memory boards which will be identical for reasons of modularity. On each memory board there will be some overhead circuitry in addition to the memory packages. Clock pulses coming from the control unit will be at TTL logic levels. These clock levels must be buffered, level translated to the 0- to 10-volt values required for the CCDs and then steered to the appropriate CCD.

The problem of driving the signals from the control unit to the memory board varies with frequency. For the "load" clocks with sampling frequency at 100 kHz, and DLM phase clocks at 33 kHz, it is quite reasonable to drive the mother board connecting the control unit to the various memory boards with CMOS devices. The voltages can be placed at 0- to 10-volt levels directly, and power benefits of CMOS can be realized without jeopardizing critical timing relationships. On the other hand, for the "dump" clocks the precharge and phase clocks occur at 21 and 7 MHz; these clocks seriously press the state-of-the-art in CMOS design. Hence, the relative signal phases for the "dump" clocks will come to the memory board at low-power Schottky levels. The "dump" clocks are level-translated at the memory board level. The clock levels should be translated at this point. Since the level translating process uses considerable power, the number of translators needs to be kept at a minimum.

Once on the memory board the number of unique lines that go to each memory package ultimately determines the density of the memory board. This results from the design criteria on spacing required at feedthrough points in a multilayer board. Therefore, the amount of steering performed at the memory board level must be elemental in order to minimize the number of different functional lines going out within the PCB. The most direct technique is to restrict the steering to either the "load" or "dump" clocks to the FIFO and LIFO CCDs. This approach is shown in Figure 28 where the clock selector performs the steering function at a CMOS level.

Using the CMOS clock selector, all CCDs within a given field memory bank will be receiving the fast clocks whenever that particular field is in the "dump" mode. Hence, a decision must be made at the package level as to when that particular CCD should dump out to the CRT. This function of passing signals to the electrodes of the CCD will be performed by the clock buffer. The title of buffer is given to this element since it is also required to drive the very large capacitive load of the CCD. This aspect of the CMOS circuitry as well as the other switching functions of the clock buffer will be discussed in Section VI.

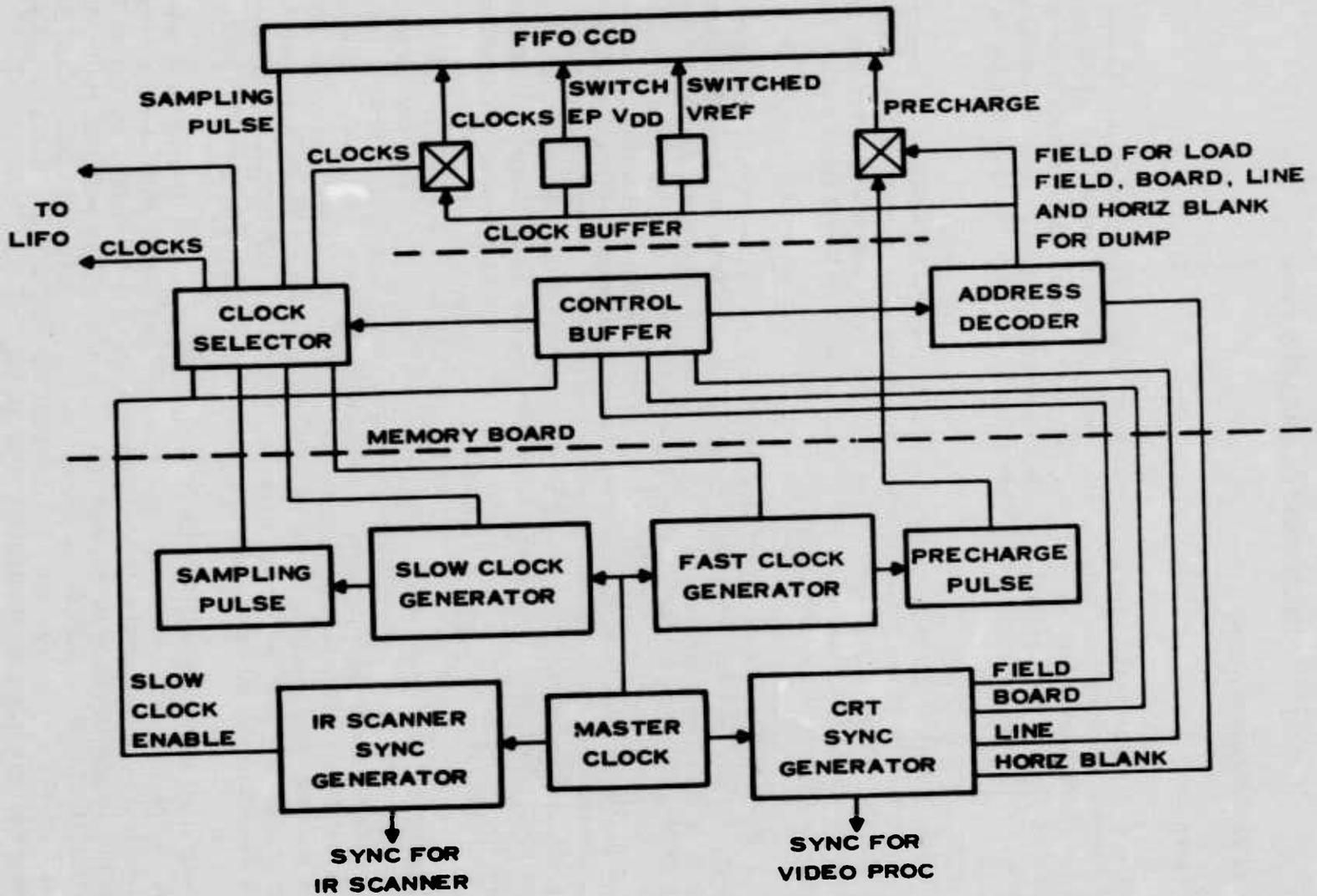

Figure 27. Schematic of Control Lines

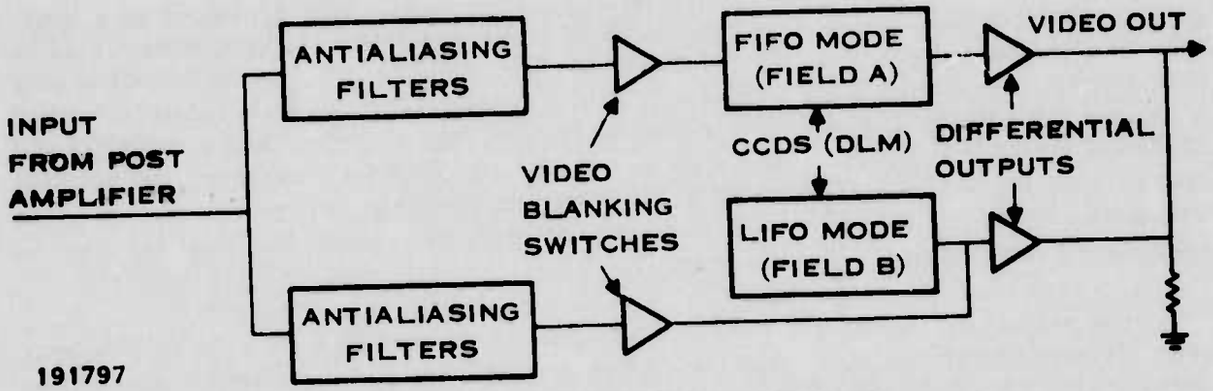

Figure 28. Functional Block Diagram of MOS CCD

2. Memory Board and Package

The two key elements in defining the exact layout of the memory board are cost and density. As will be discussed in Section IX the key cost factor is the tradeoff between chip yield and the package itself. If the number of CCDs within the package is excessive, a failure of any one of the CCD or CMOS elements can cause loss of the package and all other devices. Hence, the number of CCDs within the package should be minimal so long as the layout of the PCB does not become complex.

Another factor is that the incoming video line from each detector must be routed to two CCDs so that one can load the forward scan and the other the reverse scan. The approach which has been selected is to have the FIFO and LIFO CCDs on the same chip along with the other functions of antialiasing filters, video blanking, and differential outputs as described in the previous sections. This arrangement, shown in block diagram form in Figure 28, will minimize the number of connections from the detector-amplifiers to the image buffer elements, at the expense of having to provide both FIFO and LIFO clock connections to each package. A probable internal layout for the package is shown in Figure 29. Note that space is available for adding additional functions such as the post-amp on the MOS-CCD chip. This growth potential would not be as direct if separate packages for LIFO and FIFO modes were used.

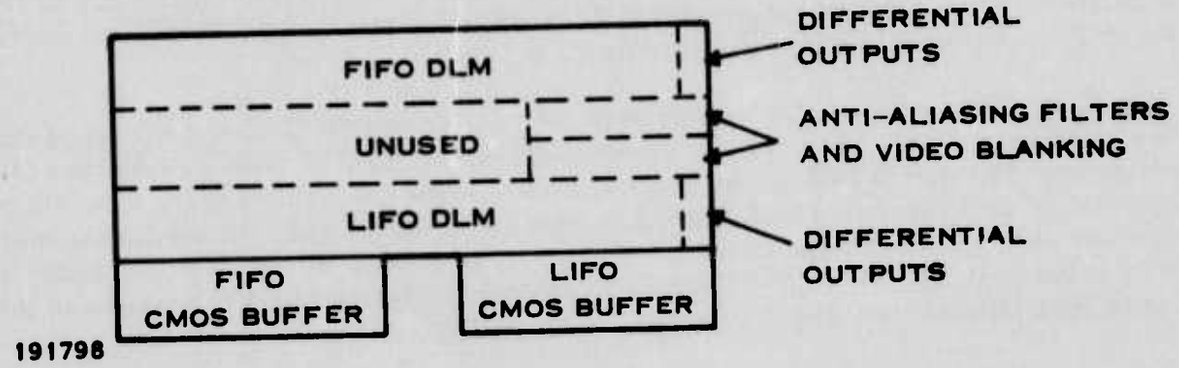

Figure 29. Internal Package Layout

More than one grouping of CMOS and MOS-CCD chips could be placed in a single package. However, due to device area and the yield versus area relations, the elements would be separate chips which were stitched bonded together. This in itself produces a yield problem on a large substrate which has a high cost factor. In this cost the dominant element in most substrates is the pin cost. Hence, the approach of placing in a package a single grouping of CMOS and MOS-CCD as shown in Figure 29 will be used. This package, called the chip carrier, will not have pins as such but solder groves. As shown in Figure 30, the chip carriers once proven to be completely functional will be mounted on a mother carrier which has pins and can be subsequently mounted to the memory board.

The number of carriers per mother carrier and the number of carriers per PCB depends upon the configuration for more than one IR line per CRT line and modularity. These will be discussed after the subsection on electronic magnification.

B. ELECTRONIC MAGNIFICATION

The memory board organization described in the section on basic configuration writes one CRT line per IR line. For some applications where the number of detectors utilized by the FLIR electronics chain becomes less than 160 and complete hands-off compatibility to the display is desired, additional CRT lines per IR line are required. This effectively expands the image that the observer of the display sees and is labeled here as electronic magnification.

The first factor to consider is that a standard CRT with 4:3 aspect ratio has an effective line to line spacing in the raster direction (vertical) of only 0.75 relative to a line. Hence, it normally overscans, which is accounted for in the MTF curves. The FLIR on the other hand performs an exact 2:1 interlace with no overlap and for the full case of 160 to 180 detectors is operated in a 4:3 aspect ratio. To understand the effect of this, consider the case of 180 detector configurations interfacing to a 525 line CRT. For 1 CRT line per IR line only 360 of the 485 active lines would be used resulting in 25 percent of the vertical display being blanked. If the complete horizontal line of the CRT were used without touching the CRT controls, the IR scene at 4:3 aspect would be presented as a 4:2.25 aspect.

There are three possible solutions to this problem: (1) increasing the output pixel rate from 21 to 28 MHz, (2) increasing the vertical gain of the CRT by a factor of 1.33 or (3) employing electronic magnification. The first approach, increasing the pixel rate to 28 MHz, is undesirable since it strains the CMOS capability and would mean only a portion of the CRT is used. Both the second and third approach are good. The vertical gain is an accessible control on CRTs and allows the image buffer to be a very simple unit for applications utilizing 160 to 180 detectors. On the other hand, in order to meet all possible detector array numbers and still fill the CRT, the technique of electronic magnification is necessary.

When writing onto the display with more than 1 CRT line per IR line, it is required that some video from the FLIR forward scan be written in the CRT field normally used for the FLIR reverse scan. The same is true for the reverse scan. This means that portions of the video will be presented to the CRT after a field delay rather than just a frame delay. This impacts the image buffer in two ways; the leadage current requirements become more stringent and the number of CCDs is increased. The effects of leakage will be analyzed in Section VIII. The remainder of this section deals with the number and organization of the CCDs.

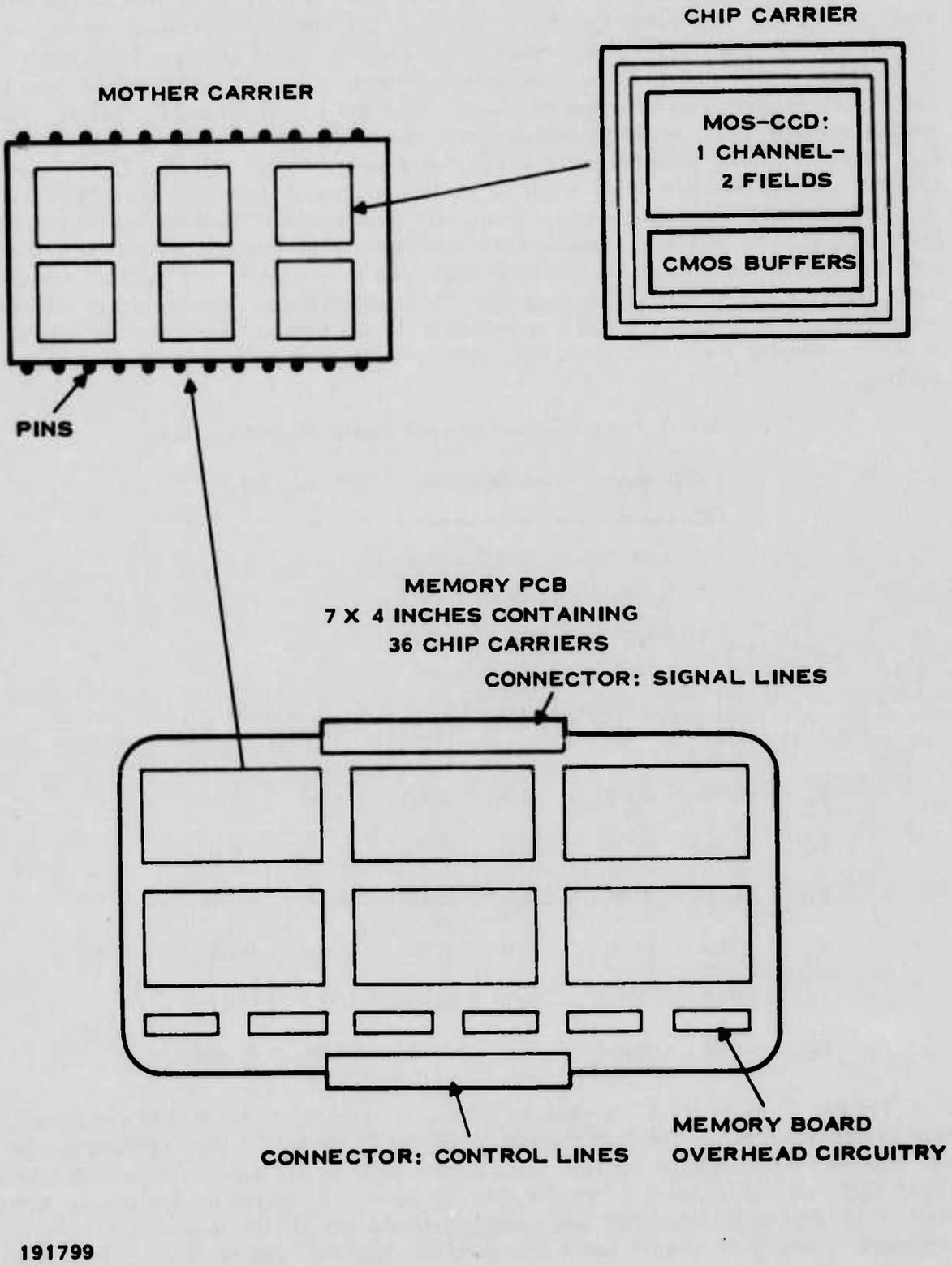

Figure 30. Packaging and Memory Board Layout

For the most direct implementation of electronic magnification, each IR detector channel will interface to six CCDs rather than two as in the basic configuration. Hence, the *ith* channel does not load just a FIFO mode CCD, F_i, and a LIFO mode CCD, R_i, in the forward and reverse scans, but F_{i1}, R_{i1} and either F_{i2}, R_{i2} or F_{i3}, R_{i3}. The relationship between the F and R symbols and FIFO and LIFO is maintained. The reason for always loading a FIFO and LIFO, F_{i1} and R_{i1}, is that any CRT line is the weighted sum of a forward and reverse IR scan line. This is done to prevent quantization or localized distortion effects. Hence, F_{i1} and R_{i1} will be handled normally at the memory board but later will be summed with R_{j2} or R_{j3} and F_{j2} or F_{j3}, respectively. The sequence for loading, storing and dumping the six CCDs of the *ith* detector is defined in Table 5. The sequence provides for always dumping a LIFO CCD, R_{i2} or R_{i3}, with F_{i1} and vice versa for the alternate or B field of the CRT. Note that the odd field CCDs (F_{i2}, F_{i3}, R_{i2} and R_{i3}) must go into a hold mode after dumping and wait to be loaded until the scanner has retraced to the proper field. This is referred to as a blank on the chart. While not using 1/3 of the CCDs, every 4th field is not optimum from the device utilization point-of-view, it is from the CMOS and packaging. If this were not done, the odd-field CCDs would be changing from FIFO to LIFO mode very 4th field and severely complicating the clocking.

TABLE 5. CCD SEQUENCING FOR ELECTRONIC MAGNIFICATION

6 CCDs assigned to each IR detector: 3 FIFO and 3 LIFO

CCD designators for *ith* detector are:

F_{i1}, F_{i2} and F_{i3} for FIFO mode

R_{i1}, R_{i2} and R_{i3} for LIFO mode

CRT designators for written field are:

A for normal IR forward scan

B for normal IR reverse scan

	A	B	A′	B′	A	B
F_{i1}	DUMP	LOAD	DUMP	LOAD	DUMP	LOAD
F_{i2}	BLANK	LOAD	HOLD	DUMP	BLANK	LOAD
F_{i3}	HOLD	DUMP	BLANK	LOAD	HOLD	DUMP
R_{i1}	LOAD	DUMP	LOAD	DUMP	LOAD	DUMP
R_{i2}	LOAD	HOLD	DUMP	BLANK	LOAD	HOLD
R_{i3}	DUMP	BLANK	LOAD	HOLD	DUMP	BLANK

The way in which the CCDs would be utilized to create a CRT line is shown in Figure 31. Four examples are given. The first example, A, Figure 31, is for the basic configuration of 1 CRT line per IR line and the odd-field CCDs are not used. In B, Figure 31, the case of 1.33 or 1/0.75 CRT lines per IR line is shown. The CRT line B_1 occurs between the forward and reverse lines of IR channel 1. Since that line normally corresponds to the reverse scan field it is comprised of odd field forward and a normal reverse field line. This is shown as R_{11}, always

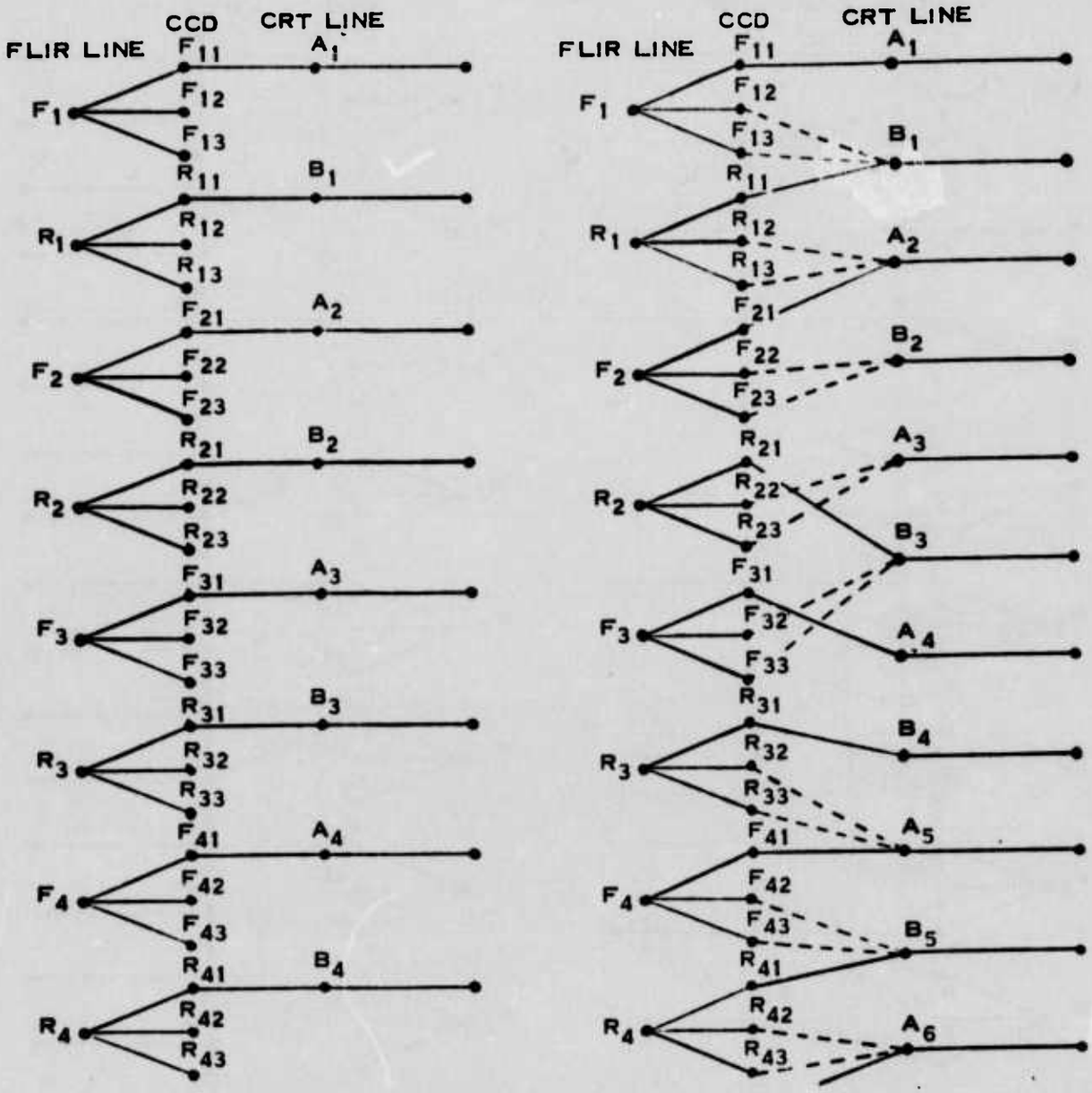

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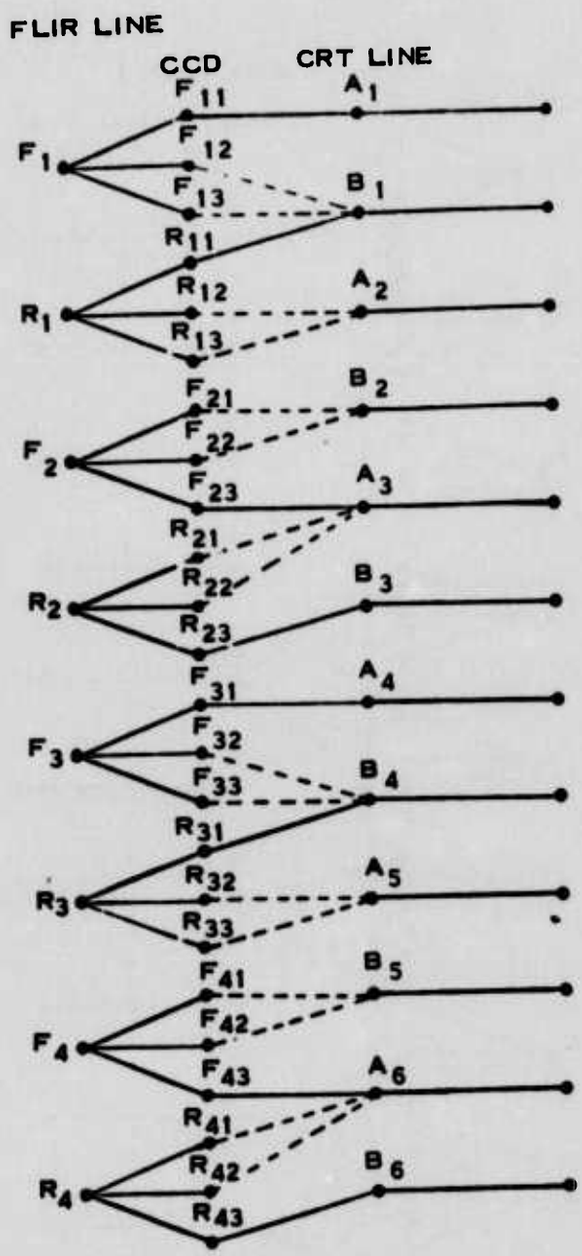
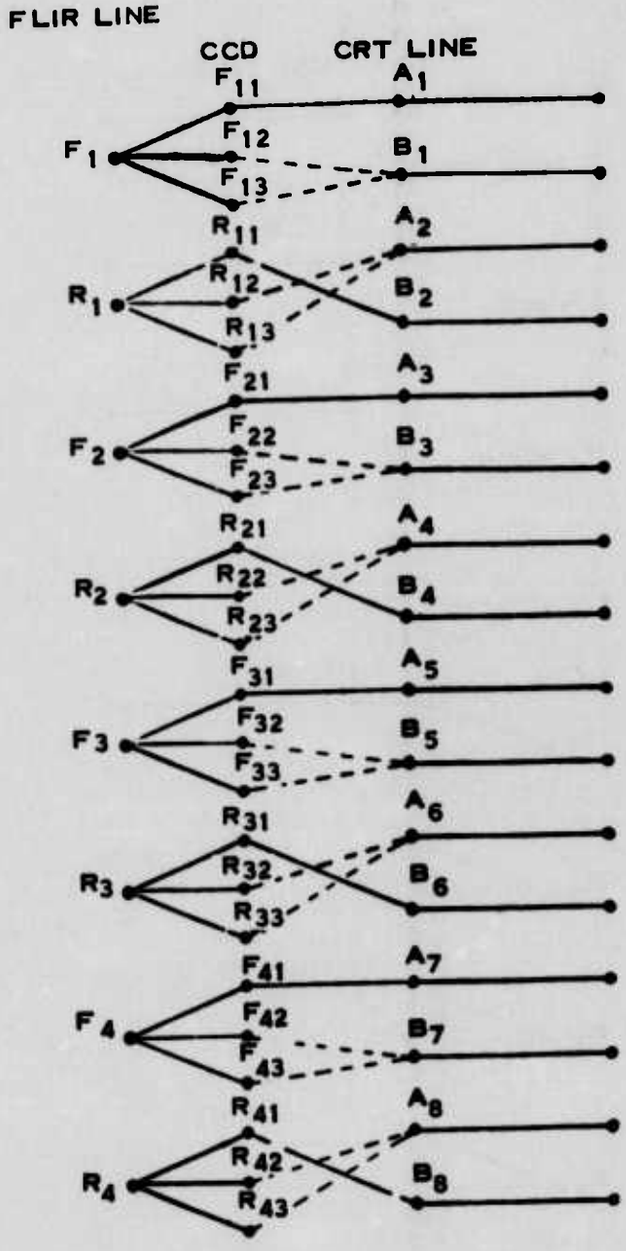
Figure 31. CCD Dump Sequencing (Sheet 1 of 2)



C. 1.5 CRT LINES/IR LINE: FILLED DISPLAY FOR 160 DETECTORS



D. 2 CRT LINES/IR LINE: FILLED DISPLAY FOR 120 DETECTORS

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Figure 31. CCD Dump Sequencing (Sheet 2 of 2)

dumping to this line, and either F_{12} or F_{13} being summed depending upon which is available according to the chart in Table 5. Note that the clock sequencing pattern starts to repeat at B_5. In C, Figure 31, and D, Figure 31, the cases of 1.5 and 2.0 CRT lines per IR line are presented in the same fashion.

This technique of electronic magnification and how it can be utilized is summarized in Table 6 where the percent of a 525 display utilized is shown. This is done for the horizontal and vertical dimensions where the variable parameters are the number of detectors and the magnification factor. There are several baseline factors involved. The output pixel rate is fixed for all cases at 21 MHz and the total pixel storage is 1080. Hence, for a 180-detector system of 4:3 aspect ratio, and sampled at 2.25 samples per resolution element is exactly filled at a magnification factor of 1.00 or 1.33. However, when a fewer number of detectors are used or a higher magnification is used, the number of samples per resolution element increases. Whenever the percent of horizontal display exceeds 100, the total FOV of the FLIR that is displayed is reduced. This is accomplished at the display by reducing the time of the load cycle.

TABLE 6. OPTIONS FOR SEQUENCING MAGNIFICATION

Baseline

CCD output clock rate is always 21 MHz

Percent of horizontal display used is determined by number of pixels stored in DLM and pixels per resolution element

Horizontal display 100 percent or less: 2.25 pixels per resolution element

Horizontal display 100 percent or more: 2.25 pixels per resolution element or more

Observed aspect ratio is unmodified when percent of vertical and horizontal display used are the same

When the percent display used exceeds 100, the display uses only the middle 100 percent in the vertical and the load cycle is decreased in time

When percent of vertical and horizontal display used are different, the aspect ratio can be preserved by increasing CRT vertical gain

Examples:

Detectors	Sequencing Magnification	Vertical Display Used (percent)	Horizontal Display Used (percent)
180	1.00	75	100
	1.33	100	100
	2.00	150	150
160	1.00	67	89
	1.50	100	100
	2.00	133	133
120	1.00	50	67
	2.00	100	100

Since the number of CCDs per channel is now increased, the channel density per memory is modified. By using the technique discussed above, the basic layout remains unchanged. The mother carrier which previously processed six channels now processes only two. The impact in terms of the number of PCBs and the actual density is shown in Table 7. Note that even with electronic magnification the density is only 2.3 inch^2/channel of the present postamplifier. This means that the total volume of the module will come out as less than the E-O multiplexer. This will be discussed further in Section X.

TABLE 7. MOTHER CARRIER UTILIZATION

- Basic Configuration
  - 1 CRT line/IR line
  - Display filled by CRT vertical gain control
  - MOS amplifiers on every chip activated
  - 6 IR channels per mother carrier
- Electronic magnification
  - Multiple CRT lines/IR line
  - Weighted sums on each CRT line
  - Display filled directly
  - Only 2 of the 6 MOS amplifiers on the mother carrier activated
  - 2 IR channels per mother carrier
- Density: 180-channel FLIR

	IR Lines per PCB	Number of PCBs	Density**
1 CRT line/IR line	36*	5	0.8 inch^2/channel
Electronic magnification	12	15*	2.3 inch^2/channel

*Both numbers are too high

**Present postamplifier density is 1.0 inch^2/channel

SECTION VI

CMOS CIRCUITS

In the previous section the block diagram of the image-buffer module was discussed. In that diagram there are two CMOS circuits which must be custom designed for this module, the clock selector and the clock buffer. The clock selector receives the incoming pulses from the control unit at TTL-levels. This chip then level translates the pulses and multiplexes them to the LIFO or FIFO CCDs. The propagation delay of CMOS depends upon the drive capability and can be as high as 30 to 50 ns on a device such as required in the clock selector and clock buffer application. Typically, the variance in propagation delay from CMOS to CMOS chip is only slightly less than the rated total. Since the time between pixels in the output video is only 49 ns, all functions of a given type must be performed on a single CMOS chip to reduce the variance. For example, the clock selector could not be made up of separate chips bonded together. Of the two circuits, the clock buffer is the most critical and will be discussed in detail in the remainder of this section.

The functional block diagram of the CMOS clock buffer is shown in Figure 32. In this figure it is seen that the various enable signals and device selection signals are used to gate the clocks and pulses to the CCD. In addition, critical dc voltages on the CCD are controlled. The schematic of the CMOS clock buffer chip is shown in Figure 33. The P/C outline is such that it is high when FIELD X BOARD X LINE is true at some point during the horizontal blanking interval. When the CCD line dump is to start, as determined when the horizontal gate becomes true, the logic allows the P/C input to feed directly through to the output. At all other times the P/C output is low.

The waveform on the output clamp gate line is the logical equivalent of $\overline{\text{FIELD}} \times \overline{\text{BOARD}} \times \overline{\text{LINE}}$. It is used to allow access to the CCD output node via the drain of the FET it controls for use as an input diode in the LIFO mode. Its use in controlling the effects of charge leakage at the output diode is described elsewhere.

The FAST CLOCK ENABLE of an earlier configuration has been replaced by its equivalent, which is generated directly on the chip. The purpose of this logic is to hold the Phase 2 line high, and Phase 1 and Phase 3 low, except when the CCD is loading or dumping. Thus, the input to the Phase 2 driver can go low, under the control of the Phase 2 input, only if either FIELD X LOAD GATE is low or if FIELD X BOARD X LINE is low while $\overline{\text{HOR GATE}}$ is low. Similarly, inputs to the Phase 1 and Phase 3 drivers can go high only under the same conditions.

The LIFO gate output is the equivalent of $\overline{\text{FIELD} \times \text{LOAD GATE}}$; it is used in the LIFO configuration to switch the input/output gate between its input and its output mode.

The circuit driving the output-drain point has the function of connecting the drain of the output FET on the CCD chip to its supply voltage V_{dd} only when the CCD is to be dumped, under the control of FIELD X BOARD X LINE. In this way the output of each CCD in the dump array is connected in turn to the common output line, without the need for further multiplexing. In addition, it reduces the power requirements, since each output stage draws power only when it is needed.

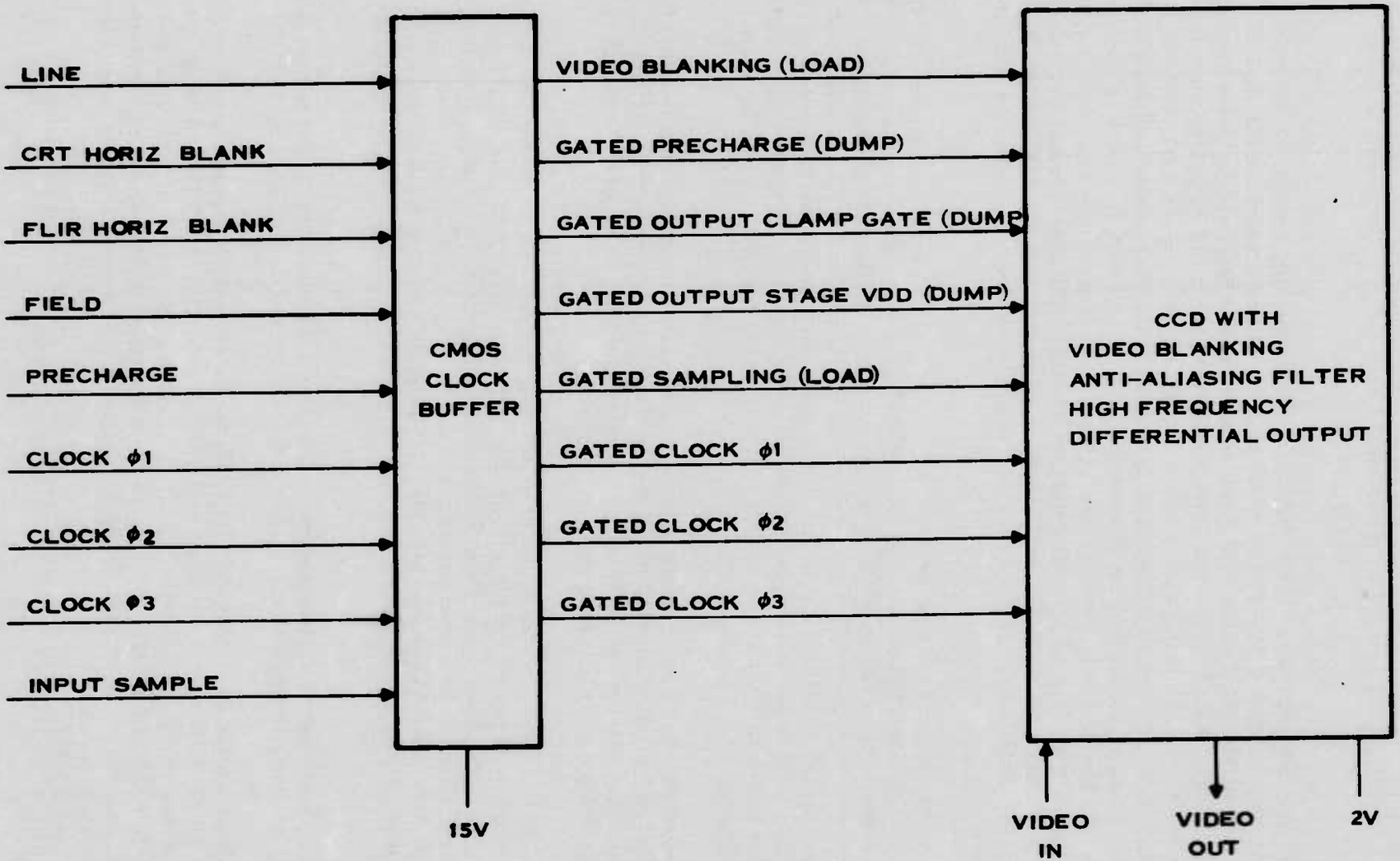

Figure 32. CMOS Clock Buffer Functional Diagram

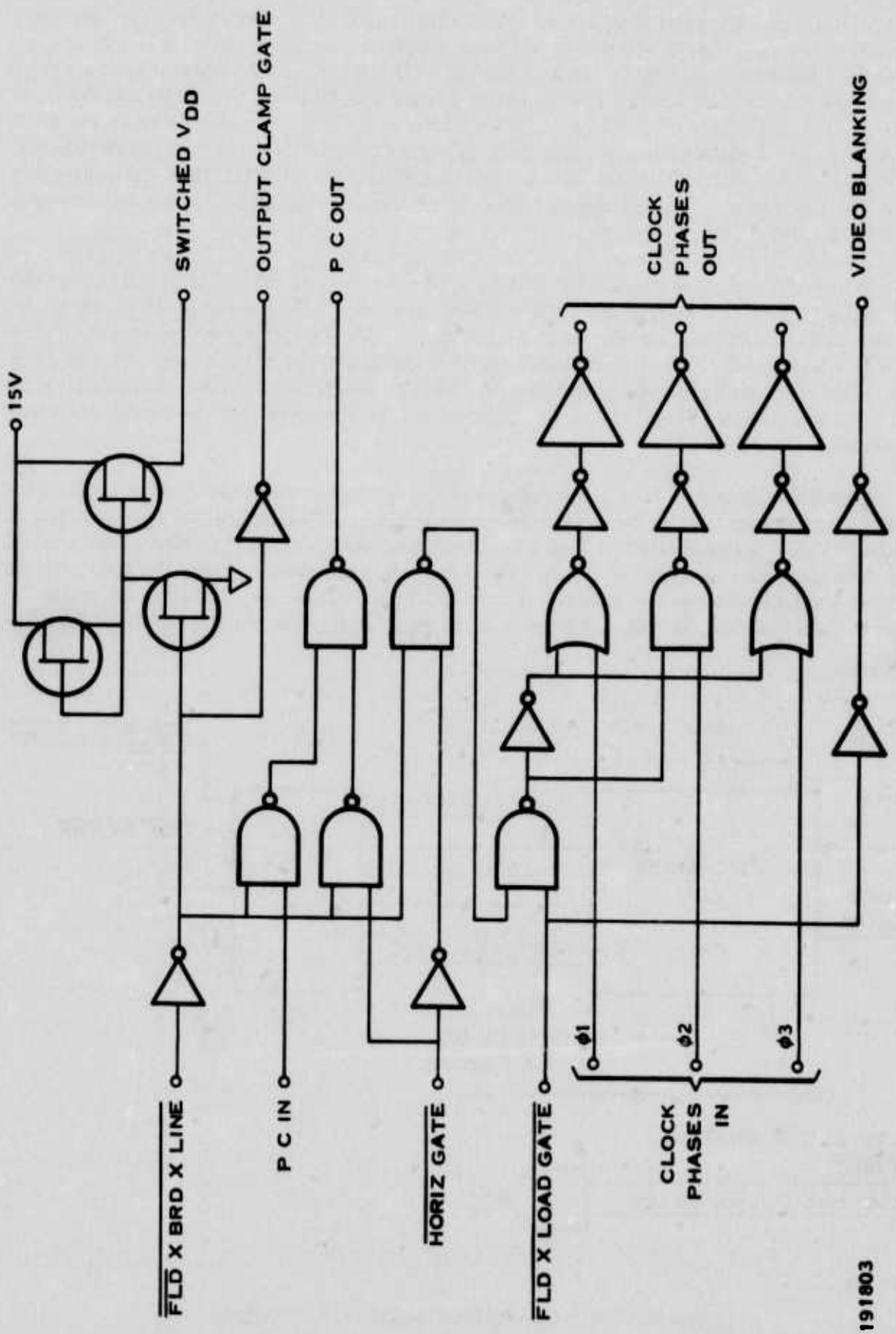

Figure 33. Schematic of the Custom CMOS Clock Buffer (for FIFO Mode)

At this time, it appears necessary to split off the sample pulse control due to requirements for a 20-volt level. This is acceptable since the timing of this slow function is not critical. Connections between the clock buffer chip and the CCD chip in the memory package are shown in Figure 34 for the FIFO mode. Corresponding connections for the LIFO mode are shown in Figure 35. The LIFO gate output from the clock buffer is not used in the FIFO mode. For both modes, the input diode sampling pulse train is gated at board level by the SLOW CLOCK ENABLE level; for the FIFO mode, this ENABLE is ANDed with FIELD. Here, the convention is that the FIFO mode is loaded during $\overline{\text{FIELD}}$ and dumped during FIELD, while the reverse is true for the LIFO mode.

Preliminary computer simulations have been run for the last version of the design for the clock phase drivers and buffers and for the CMOS stages of the precharge control system. the P/C and clock waveforms are shown in Figure 36. For the device channel widths that were selected, it was found that the clock phase rise time and fall time (20 to 80 percent) were both 13 ns, based on a load capacitance per phase of 200 pF. The precharge pulse rise and fall times were both about 6 ns. These values are incorporated in the clock and precharge waveform diagram shown in Figure 37.

Available holding-time ratio is the fraction of the total clock-out period during which there is a stabilized voltage level on the output node corresponding to the size of the charge packet. A clock-out event is completed about 1 ns after the output clock voltage has fallen to the level of the output gate, i.e., to about 20 percent above the minimum clock voltage. The hold interval can start when the clock-out is finished. It is ended, in the worst case, when the P/C pulse for the next clock-out has risen by 20 percent of its peak value. This pulse, in its turn, must be

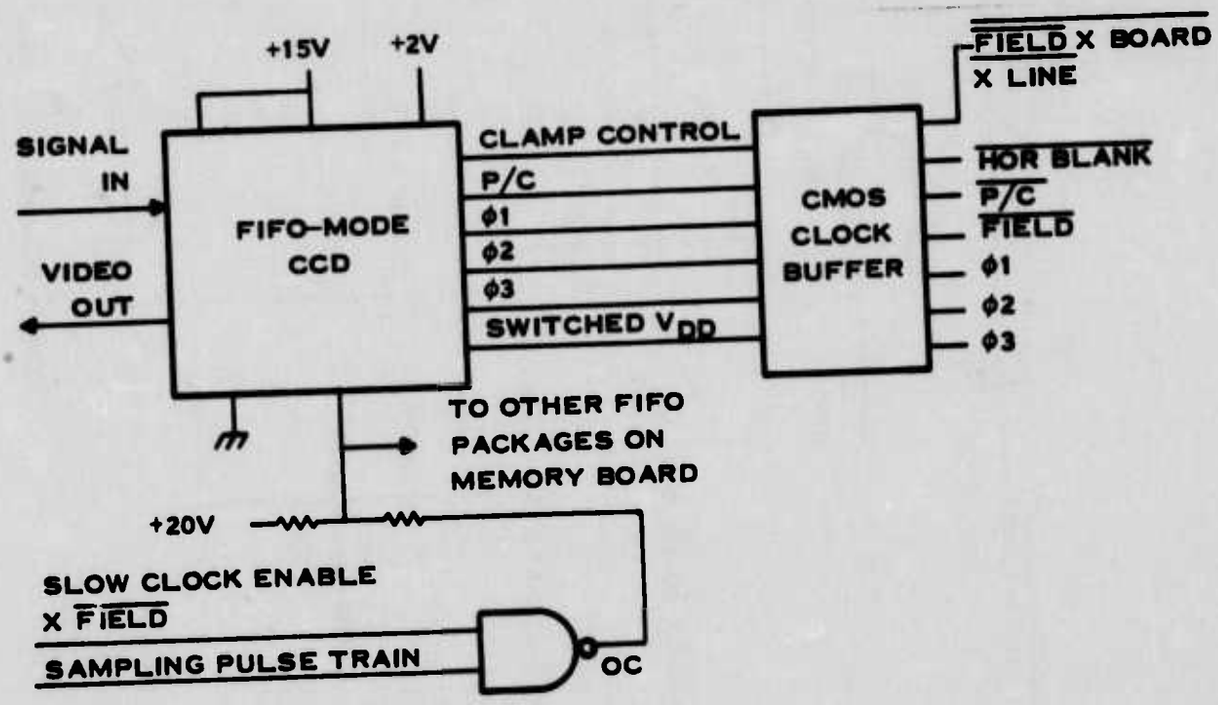

Figure 34. Clock Buffer-CCD Interconnections for FIFO Mode

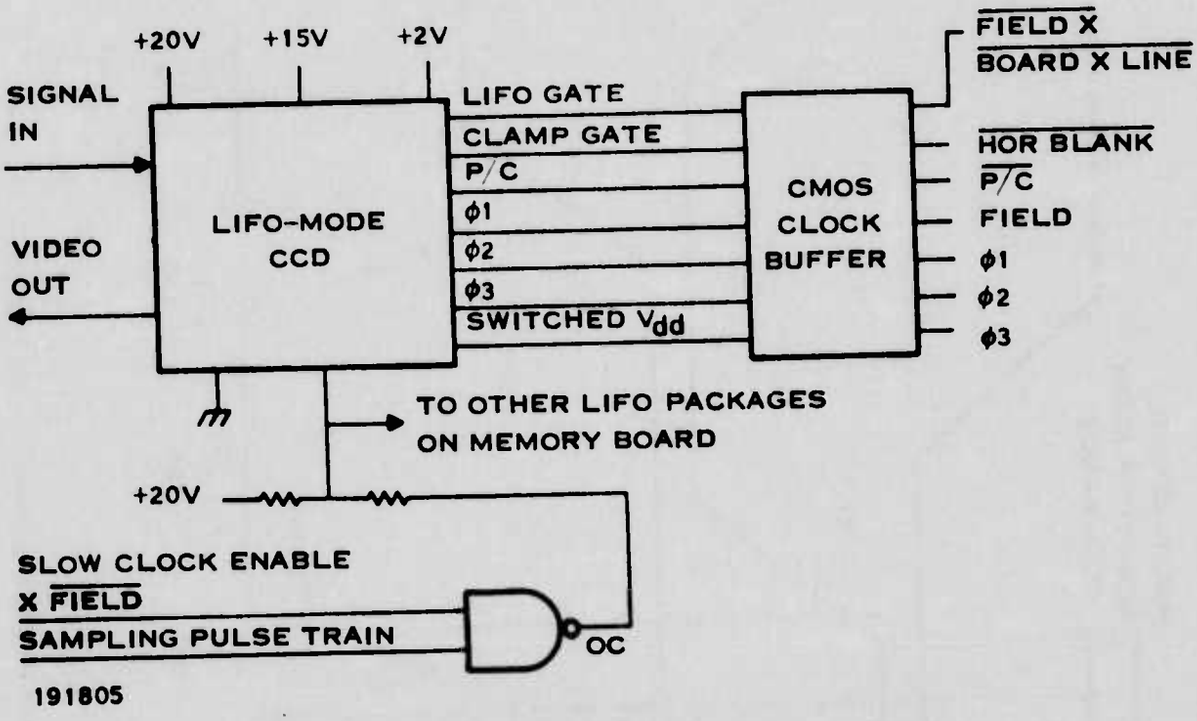

Figure 35. Clock Buffer-CCD Interconnections for LIFO Mode

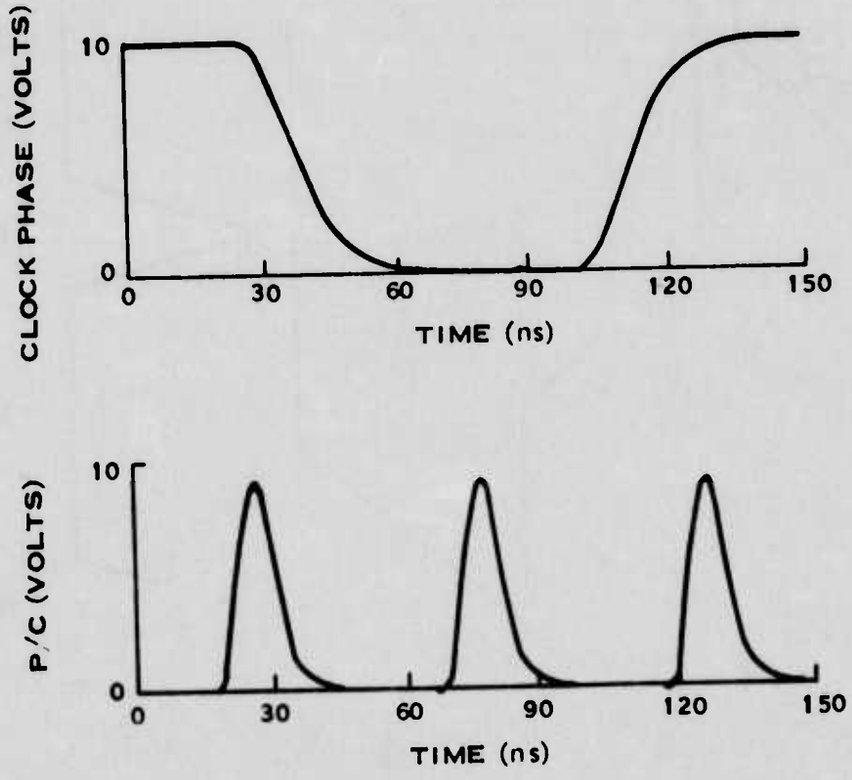

Figure 36. Computer Simulation of Clock and Precharge Waveforms

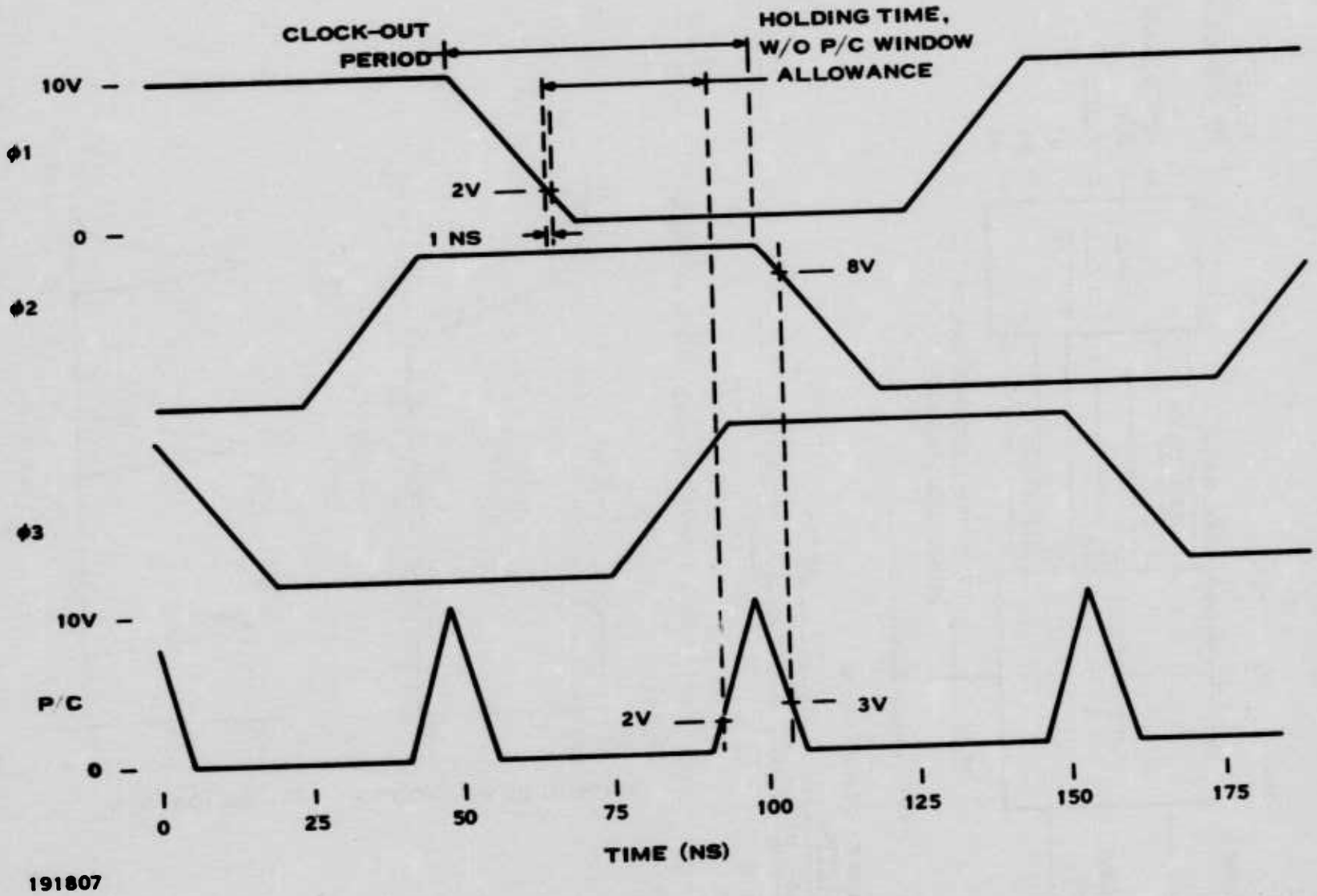

Figure 37. Waveforms for Fast-Clock Phases and Precharge Pulses

started soon enough that its fall can be completed to within 30 percent of its base value by the time the next falling clock phase has fallen by 20 percent of its total fall. These critical points are marked on Figure 36. The indicated rise and fall times of the P/C pulses and the fast clock phases were taken from the results of the simulation runs. The result is a holding time ratio of just about 50 percent. There is, of course, an additional requirement that a window of reasonable duration, say, 3 to 4 ns, be provided for the P/C pulse, relative to the clock phases. For the worst case, this leads to a ratio in the range of 40 to 45 percent.

A tabulation of the width/length (W/L) values as determined by the preliminary simulation are given in Table 8. Note that in the drivers, the P-channel transistors must have a W/L value approximately twice that of the N-channel due to their slower response for a given condition. The total size of a chip with these transistors would be 100 × 80 mils.

TABLE 8. PRELIMINARY TRANSISTOR SPECIFICATIONS FOR CMOS CLOCK BUFFER

Function	Channel	W/L	Area
Power driver	P	220	380 mil^2
	N	110	168 mil^2
Predriver	P	80	132 mil^2
	N	44	90 mil^2
Clock phase NAND	P	Minimum geometry	
	P	38	
	N	26	
	N	80	
Clock phase NOR	P	120	
	P	47	
	N	18	
	N	Minimum geometry	
Precharge output NAND	P	Minimum geometry	
	P	20	
	N	15	
	N	44	
Precharge input NAND	P	Minimum geometry	
	P	40	
	N	30	
	N	90	

NOTE: All other logic gates are constructed utilizing minimum geometry transistors.

SECTION VII
OVERHEAD CIRCUITRY

In Section V, the image buffer was defined as consisting of three subunits: the control, memory and postconditioner. The memory has been defined functionally and a layout prescribed. In this section the controller and postconditioner which interface to the memory will be discussed.

A. CONTROL SYSTEM

Figure 38 is a conceptual block diagram of the clock and the timing control for the image buffer. The master clock is to operate at 20.475 MHz. All timing for the system is to be done by two logic chains, the composite TV sync generator and the memory clocking and control.

1. The TV Sync Generator

The output waveform from the master clock is to pass through the clock phase discriminator, which will reshape the clock signal, so both logic chains will respond to the same leading edge of each clock cycle.

In the logic chain for the composite TV sync signal, the clock waveform is to be divided down by a ratio of 10 and then used to drive the input of a 3261 sync generator. Its output signals will include the even-field and odd-field control lines, the composite sync and blanking and the horizontal and vertical syncs. The even-field signal is to be used to control the phase relationships of the CCD clocks for the read-in and readout for the half of the memory elements that will comprise the first-in-first-out (FIFO) field; the odd-field signal does the same for the last-in-first-out (LIFO) field.

The composite sync and blanking signals are to be combined with the video output signals at the final output of the memory, after all the video processing stages. In addition, the horizontal sync will control the start times for turning on the fast read-out clocks to each of the CCDs in turn during the readout phase.

2. Memory Clocking

In the logic chain for the memory clocking and control network, the output from the clock phase discriminator is to be divided down to the input sample rate and then used to drive the input of the 3-phase slow-clock generator. In addition, the discriminator output will be used directly to drive the input to the 3-phase fast-clock generator. The slow-clock phases for load-in and the fast-clock phases for dump are both to be connected to the clock selector, which is part of the memory board.

The slow-clock phases will be "decoded" to provide the timing gates for the input diode pulse generator. The decoding will consist of three separate logic circuits, each providing the equivalent to the logical function, $\phi_j \times \phi_{j+1} \times \phi_{j+2}$, where ϕ_j is 1 when the *j-th* phase of the clock is high, and where j is cyclic, modulo 3, i.e., $j + 3 \rightarrow j$. The outputs of all three logic circuits are to be ORed to provide the timing gate signal. An analogous decoding will be performed for the fast-clock phases to set the timing for the precharge pulses.

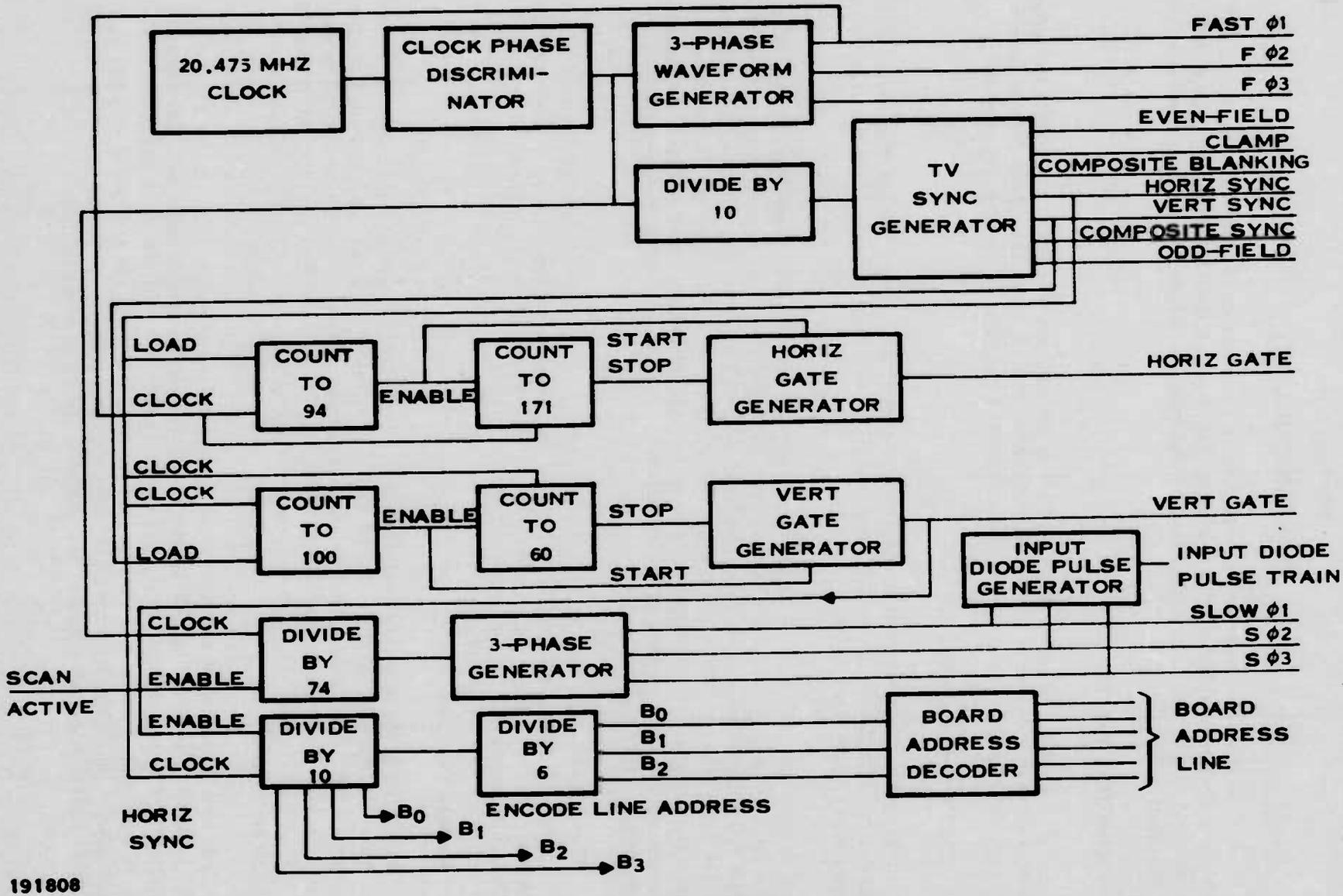

Figure 38. Schematic of Clock and Timing Control Circuits

3. Addressing the Memory Bank

Individual addresses in the memory bank are to be accessed by generating appropriate combinations of the FIELD, BOARD and LINE signals. The FIELD signal determines whether a particular memory element is to be read in or read out. Thus, memory elements in the odd field can be read into when the ODD-FIELD line is high, and can be read out when it is low. When a field is in a readout mode, a particular memory element in that field can be read but only when its particular BOARD line goes high. Once a board is selected, the particular CCD to be read out will be selected by the logic state of the LINE-ADDRESS lines. These lines, which are common to all boards, are to be decoded on each board by the decoder, which will set the line high for the selected CCD.

On the timing control board, the line and board address signals are to be generated by counting down the horizontal sync pulses. Thus, after each successive sync pulse the line address encoder will increment the selected line address count by one; when the line-address code is reset to zero, a pulse is to be sent to the board address encoder, and its output count increased by one. The encoded board address is to be decoded directly by the board address decoder, which will set each BOARD line high in turn.

Note that the BOARD ADDRESS and the LINE ADDRESS lines on each board will be active during both fields. On each board the BOARD ADDRESS line is to be responded to only if the FIELD line is set for readout. In addition, the FAST CHIP ENABLE line to the buffer for a CCD will be high only when the FIELD line is set for readout and when the BOARD ADDRESS line is high as well as the LINE-ADDRESS line for that CCD.

B. POSTCONDITIONER

1. Functions

The video output from each CCD must be brought to a common node to form a single line of video which is then fed to the CRT. In addition, the video from the CCD must be filtered to remove the precharge frequency, clamped to remove dark-current effects and adjusted in amplitude to compensate for variances in ac gain. These latter functions could be performed at the CCD level on an individual channel basis much the same way as is presently done in the present E-O multiplex concept. However, a significant reduction in components can be achieved if conditioning functions are performed on the single-line video.

A block diagram of the postconditioner is shown in Figure 39. The diagram corresponds to the case of electronic magnification. There are two identical lines of processing for the primary and secondary channels, with the two coming together for a single weighted sum at the final point of the postconditioner. If electronic magnification is not used, only the primary channel processing is necessary.

2. Summing, Filtering and Clamping

The video output from each CCD will be multiplexed to form a single-line video output. This is accomplished using series diode switching.

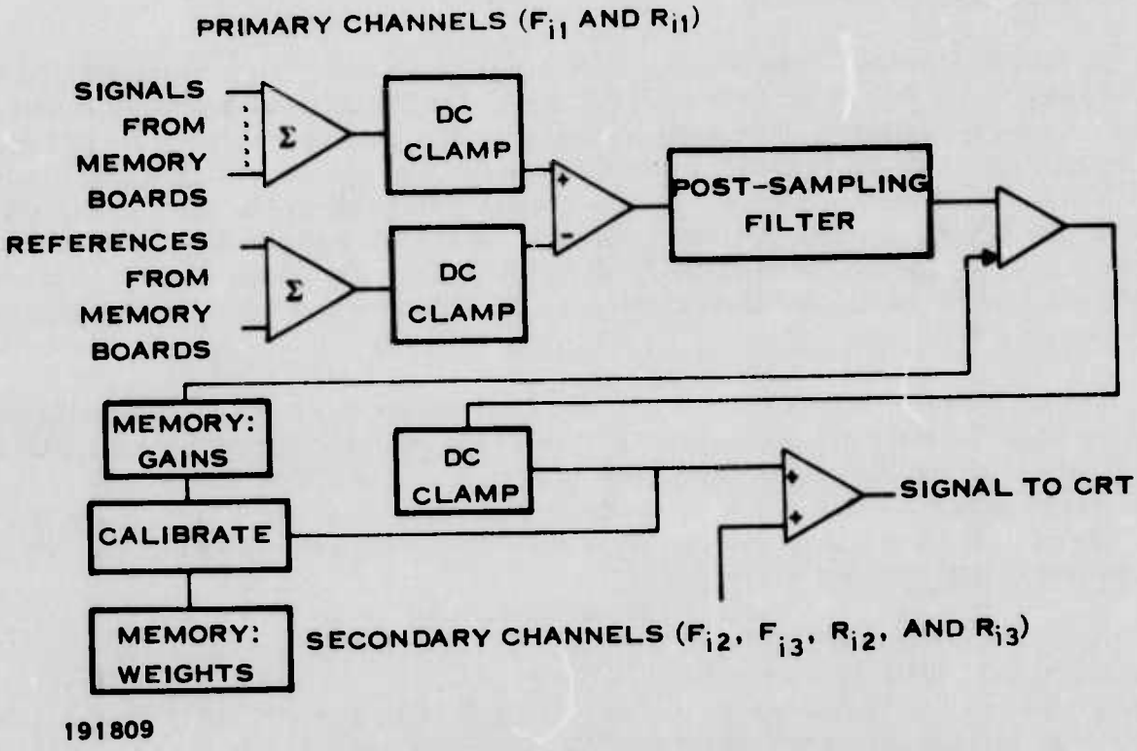

Figure 39. Postconditioner Block Diagram (Electronic Magnification)

Because only one CCD output stage is turned on at any time, a time-phased summing junction can be realized by connecting a series diode at the output of each CCD. Cathodes of all diodes on a memory board will be connected together, forming the summing junction. This single-line output will be buffered on each memory board. An identical arrangement will be used to sum the board outputs to form a single-line system output.

The summed video is then passed through a postsampling crystal filter. The filter is designed to provide a low-pass characteristic with a break frequency of $2f_o$ (9.22 MHz) (Figure 40). The CCD phase drive clocks occur at $3f_o/2$, and a deep narrow notch is designed into the crystal filter to eliminate any modulo 3 noise produced at this frequency.

To prevent the notch that is within the passband from eliminating any appreciable video information, it is made quite narrow (~5 kHz). It then becomes necessary to ensure that temperature variations do not cause the notch to drift off the $3f_o/2$ resonance. Therefore, the temperature coefficient of the crystal filter and the system crystal clock must track one another over temperature extremes of interest.

Having eliminated all video sampling noise, it is necessary to remove any line-to-line level shift that may have been caused by threshold variations within the CCD memory. This can be achieved using line-by-line dc restoration. A restoration pulse is generated during horizontal blanking for each TV line and the video information is clamped to a fixed reference level at the beginning of each horizontal line. This process removes the low-frequency component of the video which is a result of line-by-line storage. The dc restorer must be capable of restoring each

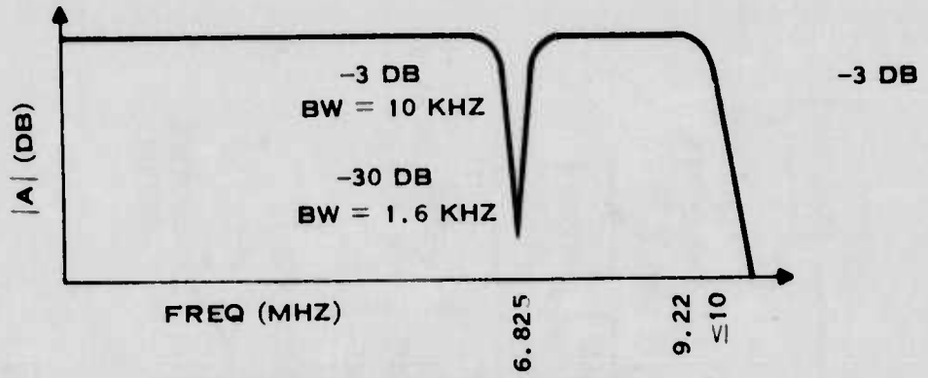

Figure 40. Postsampling Filter Specification

line of video to the same level within an accuracy of less than ½ grey shade. Video amplitude is approximately 200 mV and represents 10 gray shades. Therefore, the dc restorer must clamp each video line to within 10 mV of the reference.

3. Automatic Gain Normalization

Line scan information from all detectors of the CCD image-buffered FLIR passes through a single amplifier after being sequentially read out of the CCDs. While line-to-line uniformity could be achieved by adjusting the gain at the output of each CCD, it should be possible to automate the calibration procedure if the gain adjustment is made at the video amplifier. Calibration could then be performed in a few seconds by the operator.

The technique employs a separate gain for each stored scan line as it passes through the video amplifier. The change in gain will be made between line traces on the display, about 10 microseconds. Using this technique the normalization is obtained by storing in a random access memory the varying gains required for line-to-line gain equalization. Automatic changing of the stored gains to achieve equalization is a significant added benefit, since it can be done by an operator in the field.

C. CALIBRATION LOGIC

At the start of automatic calibration, a 20-bar target is placed in front of the FLIR to introduce a uniform periodic signal on the detectors, and the manual gain is adjusted for an average reference voltage out of the video amplifier. Figure 41 shows the automatic gain control. At the first vertical sync pulse after the calibrate start switch is closed, the address and phase-locked-loop counters are initialized. The digital gain stored in the RAM for the first video line will be sent to the input counter and to the video amplifier via the D/A converter. During the scan of the detector across the bar pattern, the signal is passed through a phase-locked loop to a demodulator. The dc level from the demodulator corresponds to the peak-to-peak level of the square-wave signal generated by the bar pattern. This dc level is compared to a reference voltage. The output of the comparator is a logic "1" is the signal is larger than the reference and a logic "0" if smaller.

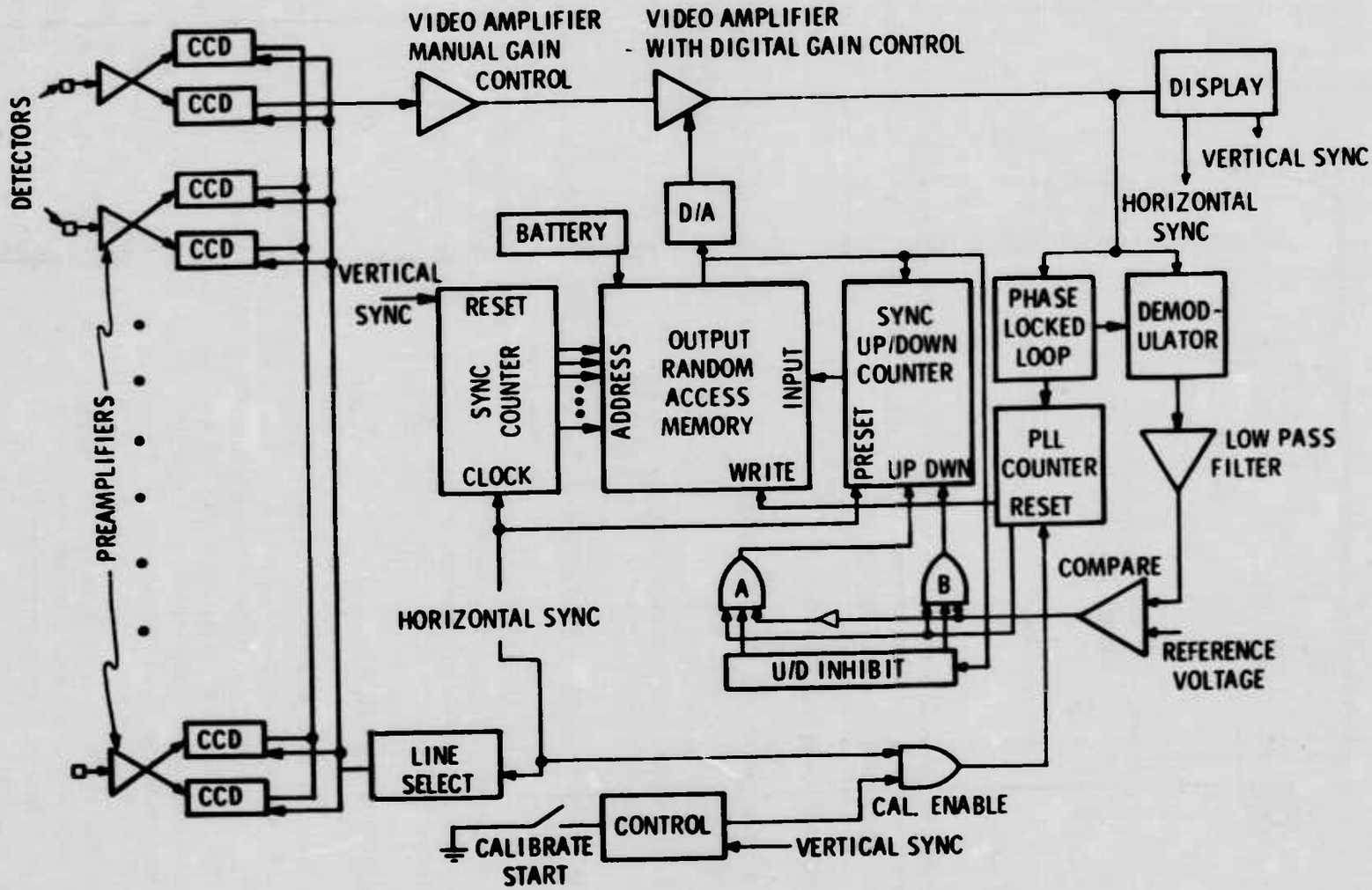

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Figure 41. Block Diagram of Automatic Gain Normalization Circuit

The phase-locked-loop counter counts the signal pulses produced by the bar pattern, and on the eighteenth pulse the inputs of "NAND" gates A and B are triggered. If a large signal is indicated by the comparator a down count is sent to the input counter lowering the digital gain by one least significant bit. The opposite occurs for an indicated small signal. On the nineteenth pulse the phase-locked-loop counter enables the write input of the RAM, and the updated information in the input counter is entered into storage.

At the end of the horizontal sweep the horizontal sync pulse updates the address counter and the cycle repeats for the next video line. When there have been enough vertical sweep pulses to allow gain steps through the full range of the RAM, the control circuit inhibits further update of the RAM, and the calibration is complete.

For a given signal placed on the detectors there will be a range of output voltages at the CCDs determined by the spread of detector responsivities, preamplifier gains and CCD characteristics. The minimum voltage, V_{min} will require the maximum gain, g_{max}, and vice versa so that

$$V_{min} \times g_{max} = V_{max} \times g_{min} = V_o$$

The gains must be adjusted to an accuracy ΔV_o determined by the number of gray shades available on the display, i.e.,

$$V_{max} \times \Delta g \leq \Delta V_O$$

therefore,

$$\Delta g/g \text{ min} \leq \Delta V_o/V_o$$

The number of gain steps necessary in each memory location is then

$$N = (g_{max} - g_{min})/\Delta g = (g_{max} - g_{min})\, V_o/g_{min}\ \Delta V_o$$

Assuming a factor of 3 for the range of detector responsivities and a 15 percent variation in gain of the preamp CCD combination, the gain range need is

$$g_{max} = 4\, g_{min}$$

For a display with 10 gray shades $V_o = 10\ \Delta V_o$, and N = 30. Therefore, 5-bit memories are needed for each video line.

D. CALIBRATION SIGNAL

The calibration signal will be generated by alternating bars of blackbody and diffuse reflector placed at the focal point of a lens. The diffuse reflection of the bars would have an effective temperature below ambient since they would reflect the housing temperature averaged with the apparent temperature of the detector Dewar in the ratio of π steradians to the angle subtended by the lens. The alternating strips of blackbody between the reflective strips could be heated if it were necessary to increase the contrast.

The calibration lens would be the size of the scanning module aperture with the bar pattern only a few inches away. The focus would not have to be good as long as it was relatively uniform for all detectors. The calibration technique is designed so that the apparent temperature difference between bars is also not critical but only needs to be within a range that the video amplifier can add sufficient gain to ensure an average output equal to the calibration reference voltage.

The scanning mirror scans the detector array across the bar pattern. The apparent temperature difference can be approximated by calculating the power difference reaching the detector from the two surfaces. The diffuse surfaces will reflect a housing temperature from 2π steradians minus the solid angle of the lens at the exit aperture. To a good approximation the radiance from this solid angle can be neglected because it will appear to be near the detector temperature.

Let:

T_c = temperature of black bars

T_a = temperature of housing

$W(T)$ = radiant emittance from a blackbody at T

E = emissivity of diffuse reflector

$F = f/D$ = f-number of lens.

The apparent radiant emittance difference as the detector is scanned across the bars is,

$$\Delta W \approx (1 - E)\, W(T_c) - (1 - E) \cos^2 (\tan^{-1} 1/2F)\, W(T_a)$$

If the f-number falls between 1 and 3 the term $\cos^2$ (arc tan 1/2F) is between 0.8 and 0.97 so that even if the bar pattern surface and the housing are the same temperature, the apparent temperature difference would be between 1.5 and 15°K (8-12 micrometers, T = 300°K and $E \ll 1$). These values fall within the nominal operating range of the system.

SECTION VIII
CRITICAL DESIGN FACTORS

In this section, all elements of the module will be brought together and interpreted in terms of performance at the display. This will be done in two parts, single-line video and two-way scan effects. The dark current is a consideration in both areas but its dominant features occur in the case of two-way scan effects. The same is also true with CTE. Hence, these CCD parameters will be discussed from the point of view of two-way scan only.

A. SINGLE LINE VIDEO

1. CCD Antialiasing Filter

The purpose of the antialiasing filter is to filter out as much as possible fo the frequency content of the incoming signal that lies above $f_s/2$, where f_s is the sampling frequency. In doing this, it should distort the frequency components below $f_s/2$ as little as possible. The ideal approach would be a sharp-cutoff low-pass filter, with a cutoff at $f_s/2$. A separate filter is needed for each CCD. For the sake of compactness, each filter is to be located on the same chip with its CCD. Because heat dissipation on the chip needs to be kept to a minimum, it was determined that the filter would be entirely passive. Limitations on the chip area available for the filter restricted the complexity of the filter to a two-pole RC design, for which the two resistances, and the two capacitances, are not far different from each other.

The transfer function for the general two-pole RC filter is

$$h(s) = \omega_o^2/[\omega_o^2 + s\omega_o^2 \{\tau_1 + \tau_2 (1 + 1/p)\} + s^2]$$

where

$$\tau_1 \; R_1C_1 . \tau_2 = R_2C_2 \; \tau_1\tau_2 = 1/\omega_o^2$$

and

$$p = R_2/R_1$$

Now the most general 2nd order filter function has the form

$$\omega_o^2/(\omega_o^2 + 2\,\delta_o s + s^2)$$

where $\delta\,\omega_o$ is the decay exponent in the time-domain solution. The particular configuration that was selected was $p = 1$, $C_1 = 2C_2$. The corresponding value of δ was found to be $\sqrt{2}$.

The filtering effects of the existing FLIR preamplifier and postamplifier were estimated as being equivalent to an identical pair of sequential, noninteracting one-pole filters, with their combined effect giving a phase shift of about 48° at f = 35 kHz. The magnitude of this transfer function is plotted as h (amp) in Figure 42, where the system fundamental frequency f_o was taken as 18 kHz.

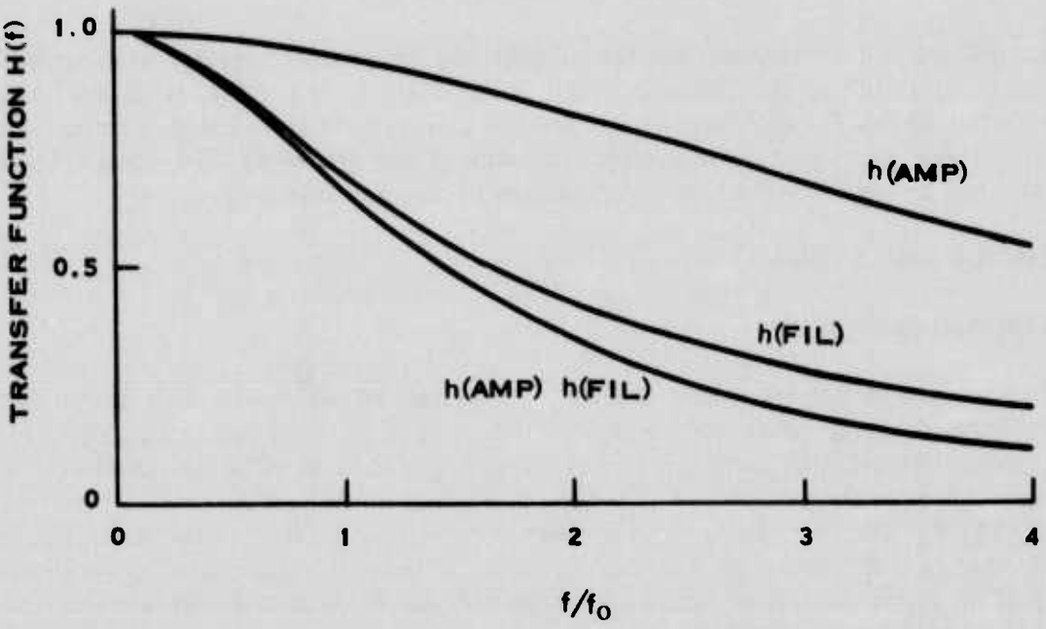


Figure 42. Transfer Functions for Circuit Elements Ahead of the CCD Sampler

Between the image buffer and the display there will be a peaking amplifier, which will be designed to compensate for the MTF loss caused by the antialiasing filter and the pre- and postamplifiers. Maximum allowable compensation is limited by the need to restrict the level of added noise, so that the detector noise is still the dominant source for the entire signal chain. Maximum compensation was taken to be about 10 dB, at $2f_o$. Thus, the minimum value for the combined transfer function h (amp) h (fil) of both filters at $2f_o$ was set at 0.35. This condition, along with the selected value of δ, determined the function h (fil) and thus the combined transfer function.

2. Variations in Clock Waveforms

In the CCD output process, one of the clock phase waveforms is assumed to have its falling edge occur late relative to the other clock phases. In this section, the effect of this on the output signal level and the fixed-pattern noise is calculated, using current system parameter values. In the worst case, the signal loss and the fixed-pattern noise are both shown to be about 3 percent of the unperturbed output signal level.

To a fair approximation, the clockout pulse waveform p(t) on the CCD output diode can be treated as a square pulse of amplitude V_{max} $(1 - 2/3\ \alpha)$; where V_{max} is the measured value of voltage change due to a maximum charge packet, and α is a charge packet size parameter. Note that $\alpha = 0$ means maximum charge packet and $\alpha = 1$ means minimum charge packet. This is represented in Figure 43. The effective stop time of the pulse is the clockout period T_s ($\simeq$50 ns), minus the precharge window ($\simeq$5 ns), minus the precharge rise and fall time, from

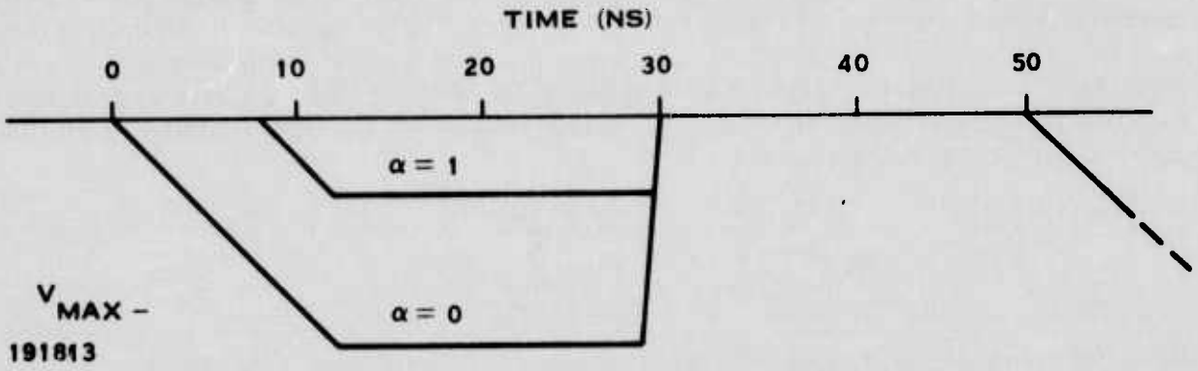


Figure 43. Typical CCD Output Pulse Waveform

3 volts on the rising edge to 3 volts on the falling edge (≃15 ns); this amounts to about 30 ns. The effective start time of the pulse is the mean of the start and the finish times for the clockout process, i.e., $\simeq(1/2 + \alpha/3)\ \Delta t(\phi F)$, where $\Delta t\ (\phi F)$ is the time for the clocking-out clock voltage to fall from 8 to 2 volts, assumed to be about 12 ns.

The size of the charge packets is modulated by the video signal amplitude. The effect of the output pulse shape on the output signal is the equivalent of flat-topped sampling of the video signal at the output pulse rate. This amounts to sampling the signal at the output pulse rate, then convolving the samples with the pulse shape

$$e_o\ (t) = [g\ (t)\ III\ (t)]\ *\ p\ (t)$$

where g (t) is the video signal, III (t) is the sampling function, p (t) is the pulse shape. In the frequency domain, this is equivalent to

$$E_o\ (F') = P\ (F')\ [G\ (F')\ *\ (1/T_s) \sum_{-\infty}^{\infty} \delta\ (F' - nF'_s)]$$

$$= P\ (F')(1/T_s) \sum_{-\infty}^{\infty} G\ (F' - nF'_s)$$

Here F′ is F/F_o where F_o is the system fundamental frequency, P (F′) and G (F′) are the spectra of the pulse and the video signal, and $F'_s = 1/F_oT_s$. By system design, $F'_s = 4.5$, while the sampling process at the CCD input effectively limited g (t) to the frequency range $0 \leq F \leq 2.25$. Thus, n = 0 is the only element of interest in determining the response to the ideal pulse shape.

P (F′) has the form P_o sinc $(\pi F'\nabla t/t_o)$, where ∇t is the pulse duration, i.e., $50 - 5 - 15 - 12(1/2 + \alpha/3) = 24 - 4\alpha$), and P_o is the impulse of the pulse, i.e., $V_{max}\ (1 - 2\ \alpha/3)\Delta t$ Even at the maximum value of 2.25 for F′, and for the longest pulse, the sinc function falls by less than 8 percent from its value at F′ = 0. In fact, the magnitude of the spectrum of the actual pulse waveform at F′ = 2.25 is rolled off by less than 10 percent from its zero-frequency value. Thus, the pulse spectrum can be approximated as flat, with amplitude P_o.

Now let only one of the three clock waveforms have a fall that is delayed relative to its precharge pulse. Then each 3rd output pulse will be short. This is equivalent to subtracting from the ideal waveform an error waveform, consisting of a short symmetrical pulse p (t), occurring once every three clockout periods. For all values of the clockout delay Δt_d, the impluse P_o of the error pulse can be shown to be $V_{max}(1 - 2\alpha/3)\Delta t_d$. When this pulse is combined with the signal waveform, the resulting spectrum is

$$E_o(F') = P'(F')(1/3T_s) \sum_{-\infty}^{+\infty} G(F - n F_s/3)$$

Here $P'(F')$ is given by $P_o \, \mathrm{sinc}\{\pi F'(\Delta t')T\}$ where $\Delta t'$ is the error pulse duration, which is generally substantially less than Δt for the values of interest. Since the sinc function is rolled off even less at $F' = 2.25$, the spectrum of the error pulse can also be approximated as flat.

Thus far, both these spectra have been calculated as time-symmetric square pulses. In reality, the error pulse should be advanced in time, so that its leading edge corresponds to the leading edge of the ideal pulse. This causes a phase shift in $P'(F')$. Combining the error pulse with the ideal pulse to obtain the actual pulse amounts to complex addition of the corresponding spectral components. For the ($n = 0$) branch of the error pulse spectrum, which is coherent with the signal, the combination acounts to a small reduction in the resulting spectral amplitude. For the worst case, the result of neglecting both the phase shift and the sinc function rolloff for the error pulse is no more than a 10 percent error.

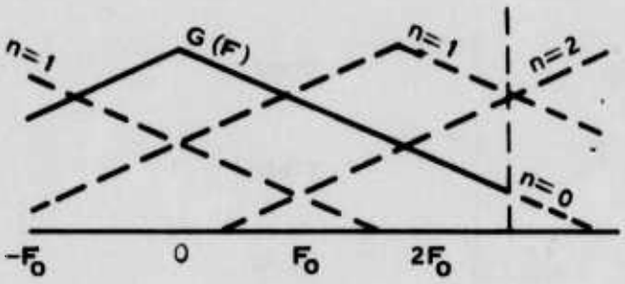
Thus, to within the error associated with these approximations, the effect of the clockout delay on the clockout signal amplitude is a fractional reduction in the amount

$$P'_o/3P_o = \Delta t_d/3\Delta t$$

Variations in the clock phase waveform propagation delay depend mainly on variations in the effective value of the threshold voltage between clock-phase buffers on the clock buffer chip. At present it appears reasonable to expect that these variations can be controlled so that $\Delta t_d \leq$ 2 ns. This will amount to a reduction of about 3 percent in the output signal amplitude.

Associated with the loss of signal amplitude is the addition of fixed-pattern noise to the signal, corresponding to all the terms $n \neq 0$ in $E_o'(F')$. The strength of the aliased noise at any frequency F' depends in general on the signal spectral components in the entire range $0 < F' < 2.25$. The way in which the various orders of aliasing contribute to the noise is shown in Figure 44. Here the line $n = 0$ shows the assumed form of the signal spectrum. Noise is folded into the passband by the branches $n = -1$, 1, and 2.

If the signal is a constant signal level, $g(t) = g_o$, and the spectrum in this case is $g_o \, \delta(0)$. Hence, only the term $n = 1$ contributes, and the noise added by the error pulse is truly modulo 3 noise, occurring at $F' = 1.5$. In general, this noise would be incoherent with respect to the signal and to the other noise components, so it would combine with these components as the sum of the squares of the amplitudes. Hence, phases of the spectral terms are of no consequence. The contribution of the clockout delay to the squared noise is



F (CUTOFF) = $F_S/2$
$F_S = 4.5F$
3-PHASE SYSTEM
G (F) IS AN ASSUMED SPECTRUM, NOT NECESSARILY REALISTIC

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Figure 44. Error-Pulse Spectral Terms Contributing to the Fixed-Pattern Noise Sum

$$\Delta [N^2 (F')] = (P'_0/3T_s)^2 \sum_{-\infty}^{\infty}{}' G^2 (F' - n F'_s/3)$$

where Σ' omits the summation over n = 0.

For the case where the input signal is a constant, the noise contribution at $F' = \Delta 1.5$ is $[N^2(F' - 1.5)] = (g_o P_o/3T_s)^2$. Spectral amplitude of the corresponding output signal is $E_o(0) = P(0) g_o/T_s$. If the modulo 3 noise were the only noise component at this point, the noise-to-signal ratio in this case would be $P'_0/3P_0$ which is just the fractional reduction in the signal level. For the same restriction on Δt_d, there would similarly be a maximum of about 3 percent fixed-pattern noise at the modulo 3 frequency $F = 1.5 F_o$.

B. TWO WAY SCAN

1. Signal Propagation Delay

The use of two-way scan with the FLIR system introduces an additional blurring of vertical edges in the field of view, caused by the different effects of signal propagation delay in the forward-scan and the backward-scan parts of the image. This two-way-scan blurring occurs for both the image buffer and for the electro-optical multiplexer forms of FLIR image processing. With the image buffer system, it is particularly easy to cancel out almost all of this additional blurring, by simple manipulation of the signal wave trains in the image buffer.

Let there be a vertical edge in the FLIR FOV. Let this edge separate two regions with uniform, different luminances. As the image of this edge is swept across the detectors, a corresponding change is produced in the detector output, and thus in the signal level that is stored in the CCDs. The FIFO CCDs are loaded in from the left of the CCD and shifted to the right, until the first sample in is at the rightmost location in the CCD. When these CCDs are dumped, the samples are shifted out to the right. Thus, the first sample in is the first one out and appears at the left end of the corresponding raster line on the display.

The signal due to the edge is actually spread out and delayed by the action of the combined transfer function of the IR optics, the detectors, the pre- and postamplifiers and the antialiasing filter. As shown in Figure 45, the optics and the detector roll the edge. However,

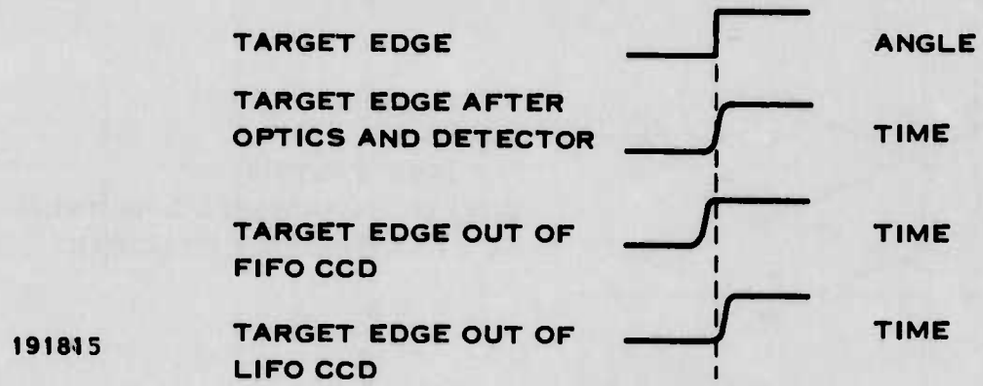

Figure 45. Component Effects on Edge Response

since the shape is produced by the convolution of a symmetric pattern with the straight edge, the center will remain at the correct edge. On the other hand, the RC components of the circuits will roll the response further and will introduce an apparent time delay.

The LIFO CCDs are loaded during the back scan of the FLIR mirror. The signal samples are loaded in from the right. During the dump, they are shifted out to the right, so that the last sample in is the first sample out and is shown at the left end of its raster line. The ideal location of the edge is the same for both scans. In the LIFO arrays, the effect of the propagation delay is to shift the edge to the right. During the back scan the step change in the object luminance is in the opposite direction. Since both arrays are dumped out to the right and painted onto their raster lines starting from the left of the display, both distributions are reversed left to right on the display.

In the current system configuration, increasing size of charge packet in the CCD corresponds to lower luminance of the associated raster line. Thus, if there is not any compensation in the two-way scan system, the sharp vertical edge of the target will appear to be blurred horizontally over a distance equal to about twice the rise-time width on either raster. The corresponding blur width for the comparable system with only one-way scan would be equivalent to only about one rise-time width. The profile of the two-way blur is indicated by the FIFO distribution minus the LIFO distribution; in the time scale of the loading process, this amounts to

$$\Delta I \left[\; 1 - E_s (t - t_o) \; - E_s (t_o - t) \right]$$

where ΔI is the final change in luminance, and where $E_s (t - t_o)$ is the step-response function for the signal chain that includes the IR optics, the detector, and the pre- and postamplifier and the antialiasing filter. The edge response for total electronic transfer function is shown in Figure 46 for the LIFO and FIFO cases. It is clear that the peak amplitude and the extent of the vertical blur profile could be reduced if the two distributions can be shifted so that their overlap is improved. This amounts to shifting the LIFO branch of the blur with respect to the FIFO branch. The form for the difference function then becomes

$$\Delta I \left[\; 1 - E_s (t - t_o) \; - E_s (t_o + t_d - t) \right]$$

where $t\lambda$ is the relative delay of the LIFO line, corresponding to a rightward shift.

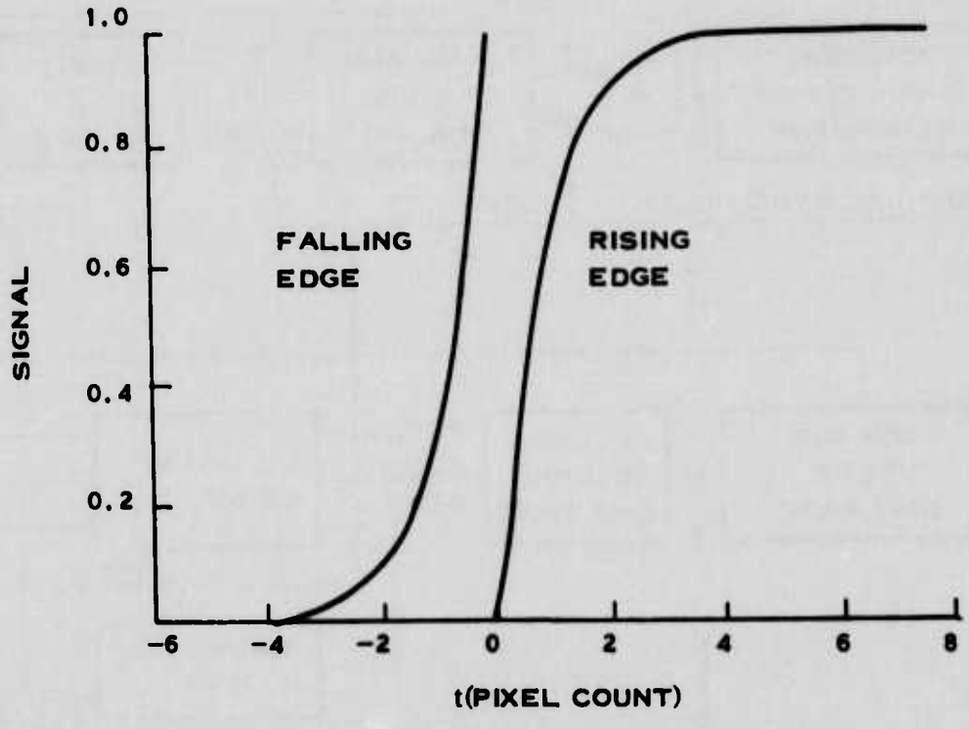

Figure 46. Electronic Edge Responses for LIFO and FIFO

The shifting can be done in several equivalent ways, by shifting the effective position of either the FIFO or LIFO signal trains, during either the load or the dump process. The present plan is to continue the LIFO loading process until the LIFO signal is displaced leftward by the required integral number of pixel positions. Then, when the LIFO lines are dumped, the fast LIFO clocks will start the dump at the same relative time as do the fast FIFO clocks, and the LIFO signal train will be effectively delayed by the required number of pixel positions.

The LIFO loading process can easily be extended, as shown in Figure 47 by adding the interger i to the total count N of slow-clock cycles that are required before the slow-clock generator is turned off at the end of the LIFO loading. At the end of the slow-clock waveform, the charge packets are made to end up at the phase 2 electrode positions, regardless of when during the previous three-sample-pulse interval the stop signal arrived. For this reason, the train of signal samples in any one channel of the CCD can be displayed only by integral pixel positions.

The smallest interval of delay compensation that can be provided in this way is 3 times the sample interval. Smaller amounts of additional compensation can be achieved in 2 successive steps, as shown in the sketch. At the end of the starting delay for the LIFO slow clocks, the (÷M) pulse train is delayed by a selectable count of 0, 1 or 2 pulses, corresponding to an additional delay of this many sample-pulse intervals. Then a variable-delay one-shot provides a final increment in the clock delay, of a continuously variable amount up to one sample-pulse interval.

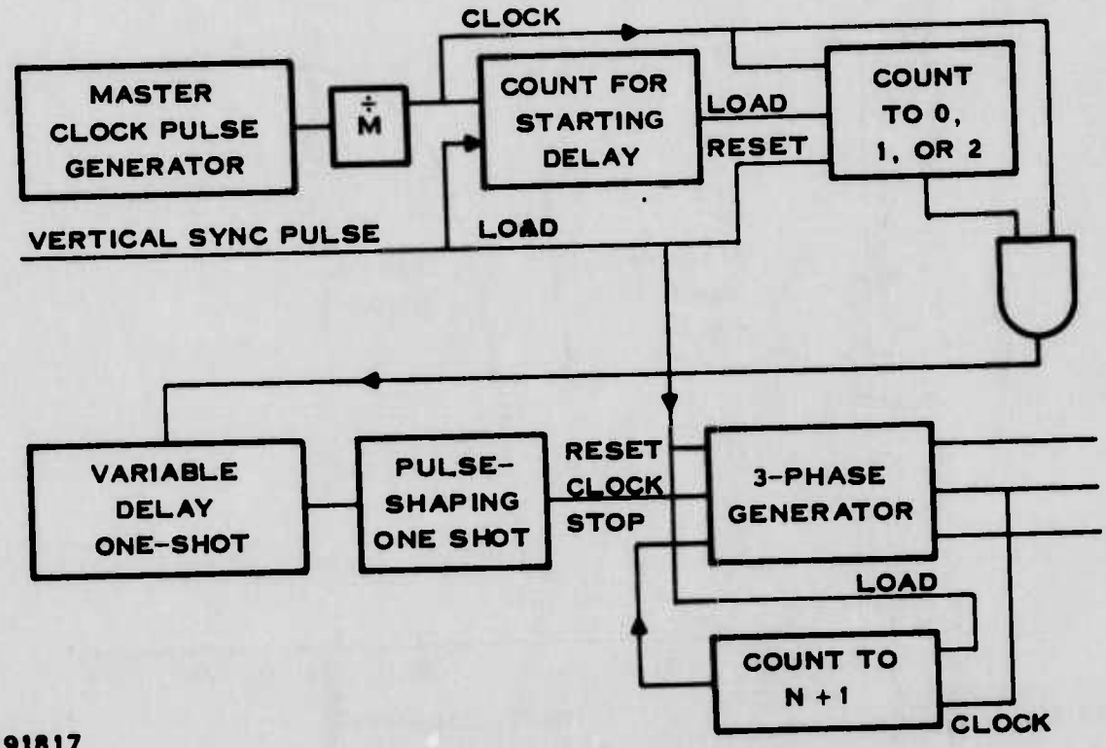

Figure 47. LIFO-Mode Delay Compensation Circuit

Thus, the total LIFO delay is achieved by delaying the slow clocks by both integral and fractional sample intervals, and by displaying the LIFO samples leftward in the CCD, in units of one pixel interval of three sample intervals each.

Note that the configuration shown in the sketch is the modification to the slow clock generator appropriate for adding the LIFO delay. It would be possible to provide separate slow-clock generator chains for LIFO and for FIFO. A preferable alternative would be to switch around the count-to-0, -1, -2 circuit and the one-shots when the FIFO CCDs are to be loaded, using a switch operated by the FIELD logic level. Here FIELD would also be used to toggle the slow-clock count requirement between N and N + i for FIFO and LIFO loading.

A calculation was made of the system response to a unit step input; the calculated response was used to show more exactly the amount of reduction in the FIFO-LIFO blur that could be obtained by optimal LIFO delay. The transfer function used in finding the step response included the diffraction and blur of the IR optics, the cutoff due to the detector width, and the characteristics of the detector-amplifiers and of the antialiasing filter. The step response was calculated by a term-by-term summation of the Fourier-series terms of a long-period square wave, each term being modified by the appropriate value of the transfer function. The result is shown in Figure 48. Included in this step response for the system is the peaking function which compensates for the antialiasing filter. The time is in units of the sampling interval. Thus, the corresponding profile of luminance along the display raster lines can be determined by noting that 2.25 sample spacings corresponds to the spacing between successive interlaced raster lines. Figure 49 shows the superposition of FIFO and LIFO step responses, with optimal effective delay of the LIFO waveform. For this step response, the optimal delay is about 2.2 sample

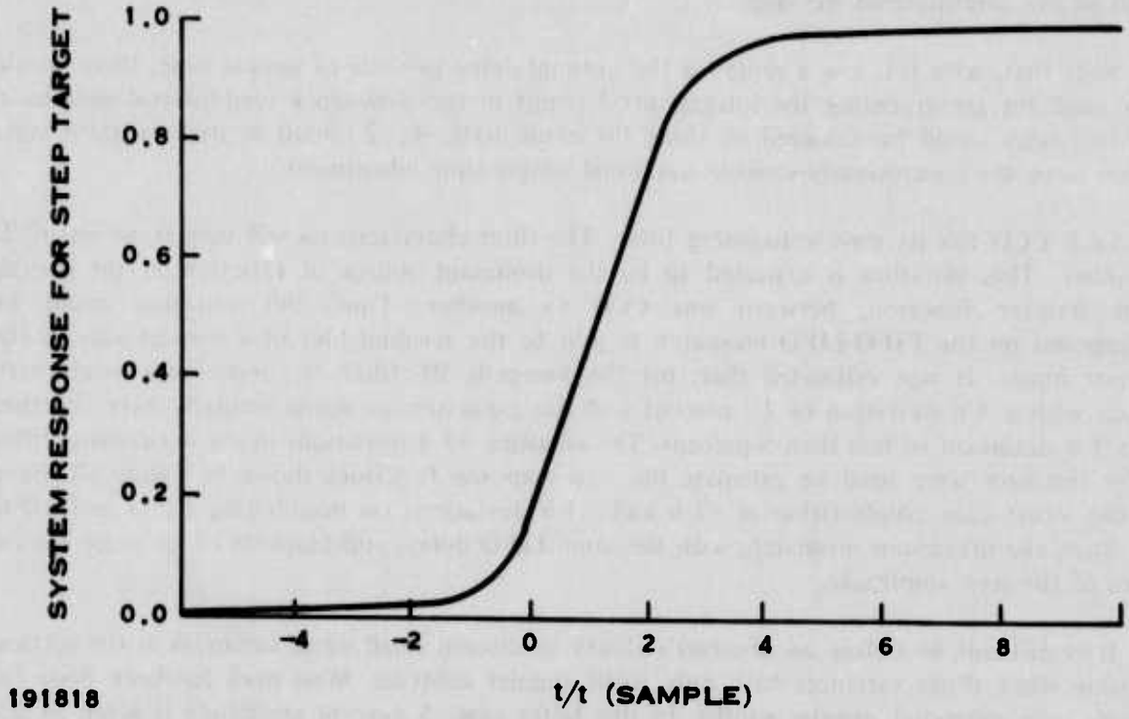

Figure 48. System Edge Response for FIFO Channels

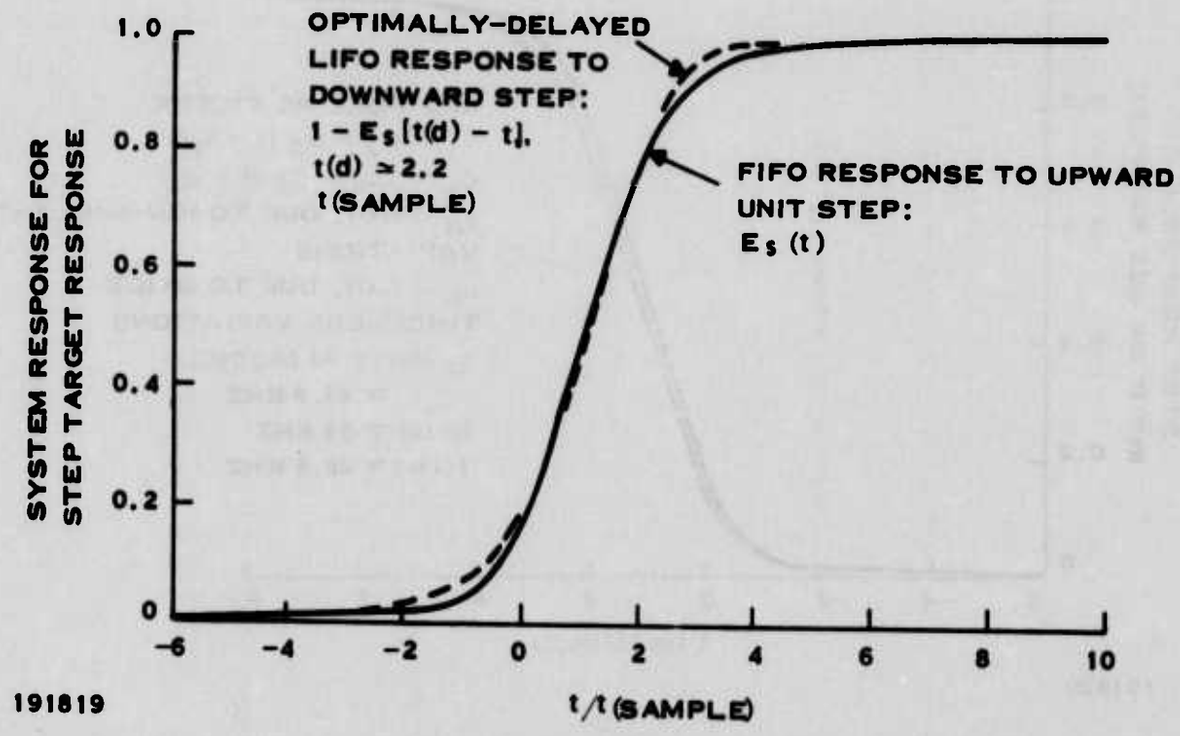

Figure 49. Optimal Match Between FIFO and LIFO Step Responses

intervals and the maximum residual mismatch between the FIFO and LIFO profiles is about 3 percent of the amplitude of the step.

Note that, with this low a value for the optimal delay in units of sample time, there would be no need for incrementing the integral pixel count in the slow-clock load-interval generator; the entire delay could be achieved by using the count-to-0, -1, -2 circuit in its two-count state and also using the continuously-variable fractional-sample-time adjustment.

Each CCD has its own antialiasing filter. The filter characteristics will vary from one CCD to another. This variation is expected to be the dominant source of variation in the overall system transfer function, between one CCD to another. Thus, this variation could be superimposed on the FIFO-LIFO mismatch to add to the residual blur of a vertical edge in the displayed image. It was estimated that, for the two-pole RC filter, the resistances would vary together with a 1 σ deviation of 10 percent and the capacitances would similarly vary together with a 1 σ deviation of less than 5 percent. The resulting $\pm 1\ \sigma$ deviations in the antialiasing filter transfer function were used to calculate the step response functions shown in Figure 50. Even with the worst case combination of $+1\ \sigma$ and $-1\ \sigma$ deviations on neighboring FIFO and LIFO raster lines, the maximum mismatch, with the same LIFO delay, still amounts to no more than 6 percent of the step amplitude.

It is difficult to define an observer's ability to discern small signal variances in the vertical dimension when those variances have only small angular subtense. Most work has been done for variances over extended angular widths. In this latter case, 5 percent amplitude is given as the minimum perceptible level. If the amplitude variance in Figure 49 is placed in an area context,

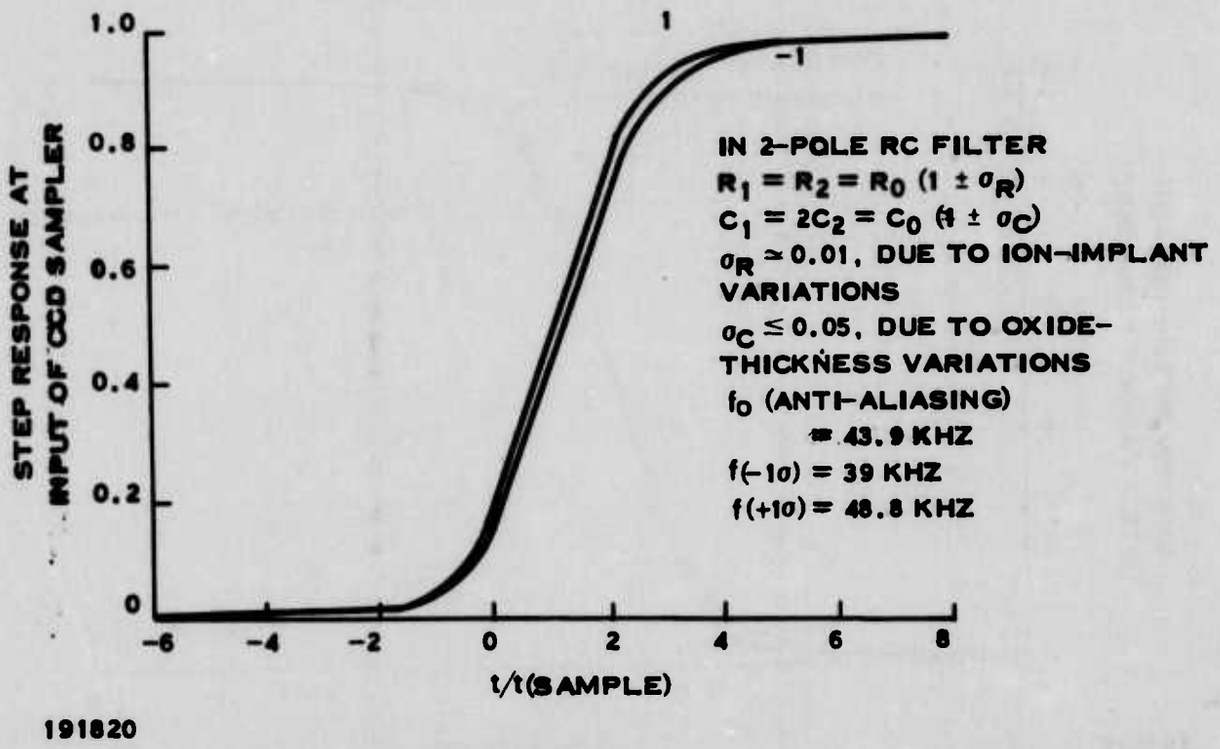

Figure 50. Effect of Variations in Antialiasing Filter on FIFO-LIFO Mismatch

the difference in LIFO and FIFO becomes 1.8 percent in a resolution-element width. If this interpretation is used, the variance is well below the 5 percent value and the resolution element is also small. Thus, it was concluded that in a system with two-way scanning, optimal delay of the LIFO signals with respect to the FIFO signals will reduce the additional blurring to an insignificant level, both in extent and in amplitude.

2. Charge Transfer Inefficiency

Charge transfer inefficiency in the CCD image buffer is considered as an additional source of mismatch between neighboring raster lines in a two-way scan system. This effect is combined with signal-propagation delay; the resulting mismatch is judged not to have a significant effect on the appearance of targets in the display or on the detectability of these targets. This judgment makes use of the present CTE values of better than 0.9999 which are now routinely attainable.

In the previous section, the additional blurring of vertical edges in the displayed image, arising from the use of two-way scan and the effect of signal propagation delay in the circuitry ahead of the image buffer was considered. Here the further contribution to the blurring in a two-way scan system, due to the non-negligible charge transfer inefficiency in the CCD is included.

Assume that the sampled signal at the input of the CCD has the form $q_o(t')$, where t' is in units of the time interval between successive charge packets in a single channel of the CCD. After M transfers, the size of the charge packet, now at the M-*th* location in the CCD, is given by

$$qM(t') = (1 - \epsilon)^M \; [q_o(t') + M \epsilon \, q_o(t' - 1)] + \frac{M(M + 1)}{2!} \epsilon \, q_o(t' - 2) \ldots$$

where ϵ is the charge-transfer inefficiency. Thus, a charge packet changes with time as it moves through the CCD only if it follows closely after a change in the input signal level.

Assume that in the FLIR FOV there is a target that is scanned both in the forward and backward scan directions. Let it be a uniform target with sharp vertical edges, so that the corresponding waveform, as it is loaded into either the FIFO or LIFO CCD, is a sharp-cornered square pulse. Here, we temporarily neglect the unit-step response function, as derived in the previous section, in order to clarify the qualitative effects of CTI in producing a difference between the FIFO and LIFO parts of the image. On the forward scan, the pulse is loaded in on the left and clocked part of the way along the CCD during load. During dump, the pulse is clocked in the same direction the rest of the way along the CCD to the output. For the fast-clock rates of interest here, and all lower rates, the value of ϵ is not significantly dependent on clocking rate since the clock rate is kept below 10 MHz. (In a three-register DLM which has an output pixel rate of 21 MHz clock rate.) Thus, regardless of where in the FIFO CCD the pulse pattern is located after the load process, the shape of the pulse at output is the same, with rounding at the leading corner and a decay pattern after the falling edge. This is shown diagrammatically in Figure 51.

When the same square pulse is loaded from the right into the LIFO CCD, the same kind of rounding and decay pattern develops on the signal profile as the pulse moves leftward. When the pulse is clocked out, however, the direction of motion is reversed; an additional rounding and decay pattern develop on what is now the leading and the falling edges. The rounding that develops on the upper right hand corner during dump is slightly different from the rounding that

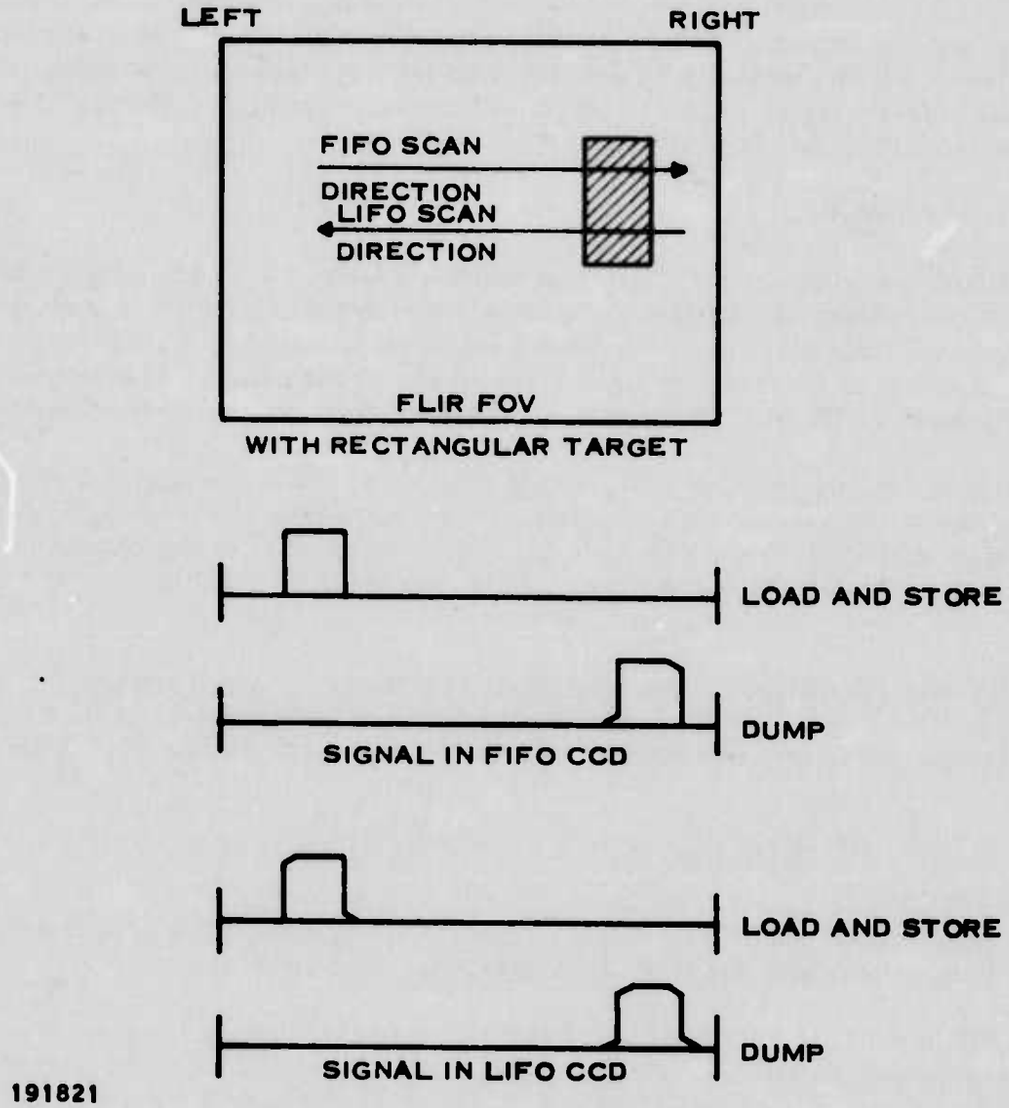

Figure 51. Diagram of CTT Effects in Two-Way Scan Operation

had developed on the upper left corner during load, because the size of the differences across the edge of the pulse is slightly less. At the same time, the rounding and decay produced during loading is itself slightly attenuated. Note that for a target in the far left side of the FOV, the CTI effects will be completely negligible in the LIFO CCD.

The net charge is not lost but effectively displaced only some during the charge-transfer process. As shown in Figure 52 the total amount A_2 of charge lost from the front edge of the FIFO pulse must equal the amount A_1 of charge gained at the falling edge of the pulse. For the case of the initially sharp-cornered pulse, it can also be shown, by a term-by-term comparison, that the shape of the regions A_1 and A_2 is the same, if the approximation is made that the width of the pulse is very short relative to the distance the pulse has been moved through the CCD.

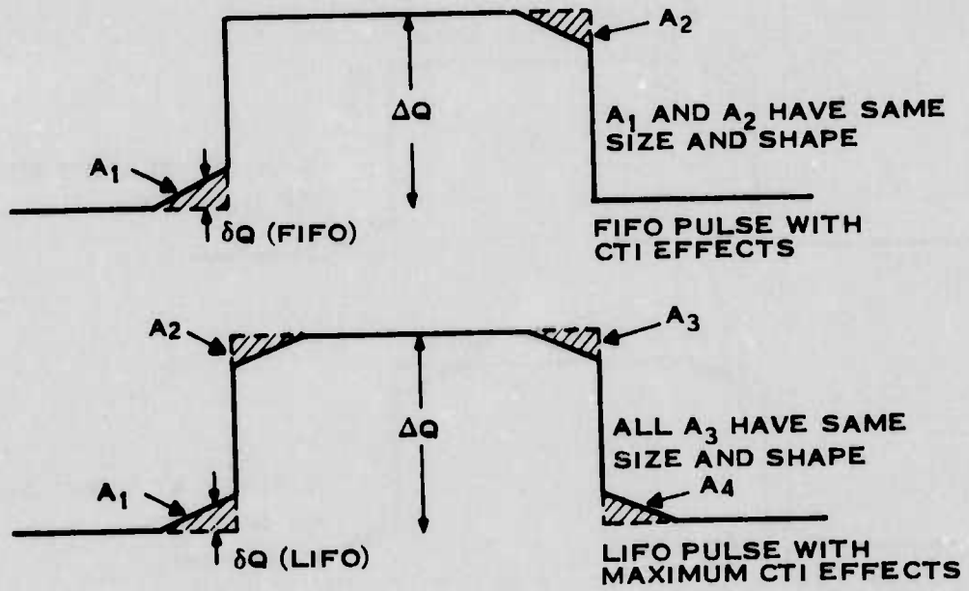

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Figure 52. CTI Effects on Square Signals for LIFO and FIFO Modes

Similarly, it can be shown for the LIFO pulse at the output that all the areas A_i have the same shape and size. The size of the As for the LIFO CCD depends on the amount that the pulse was moved into and then out of the CCD. This, in turn, depends on the horizontal position of the target in the FOV. For a target at the left edge of the FOV, there will be essentially no CTI effects on the pulses; the effects will be maximum for a target at the right edge of the field. Even in this latter case, the net strength of the effects is less than for the FIFO CCD.

The mismatch between the luminance profiles for the same pulse as appearing on neighboring LIFO and FIFO raster lines is likewise a function of the location of the target in the FOV. As shown in Figure 53 the greatest mismatch occurs for targets at the left edge of the display; there the amount of the mismatch corresponds to the total FIFO CTI effect.

Even when allowance is made for the step-response function for the system elements ahead of the CCD, it is still true that the worst case contribution to the FIFO-LIFO mismatch is for targets at the right edge of the FOV. Thus, a comparison of a LIFO step response without CTI effects, with a corresponding FIFO step response with full CTI effects, will show the largest CTI contribution to the mismatch and, thus, to the amplitude of the blurring of the vertical edges of the target.

The FIFO step response was calculated and then convolved upon itself to include CTI effects. The formula given above for $q_M(t')$ as a function of $q_0(t' - i)$ was used in these calculations. As noted earlier, the unit step in i corresponds to three sample times, since only every 3rd sample is entered into a particular channel of the DLM CCD. The resulting changes in

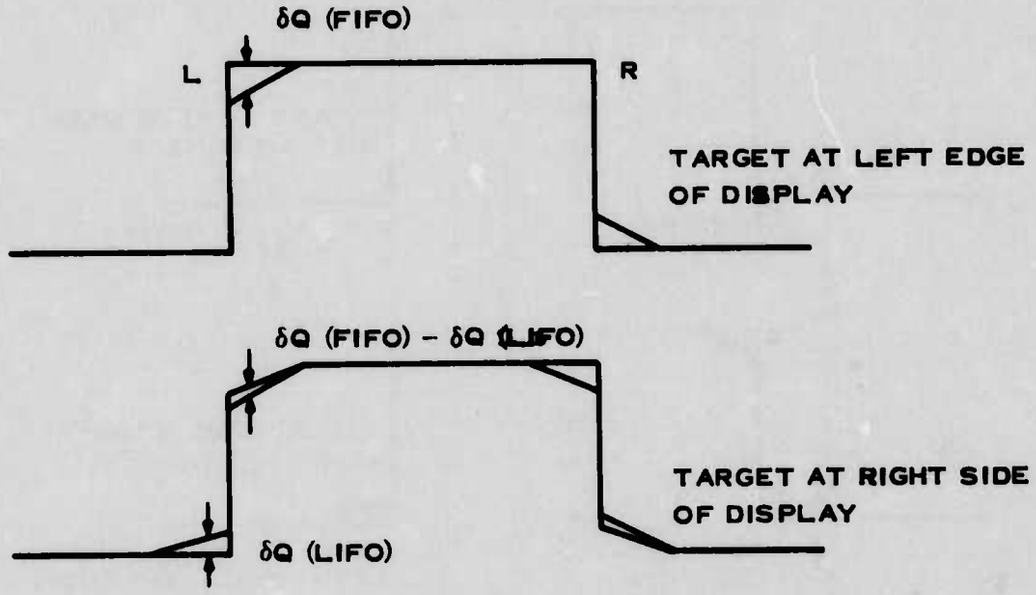

Figure 53. Differences Between FIFO and LIFO Pulses

the step response are shown in Figure 54 for the CTIs of interest in this application. These curves have been overlaid with the LIFO curve without CTI effects. The resulting values for the optimal LIFO delay, in sample times, and for the maximum FIFO-LIFO fractional mismatch are given in Table 9.

TABLE 9. FRACTIONAL MISMATCH VERSUS CTI

CTI	CTE	Optimal Delay (Pixels)	Fractional Mismatch (Of Full Signal)
0.0	1.00	2.2	0.03
5×10^{-5}	0.99995	2.4	0.06
7×10^{-5}	0.99993	2.5	0.07
1×10^{-4}	0.9999	2.6	0.08

These values of mismatch are expressed as fractions of the amplitude of the unit step. The amplitude of the charge packets is converted on output to voltage into the video processor. This modifies the voltage levels going into the CRT so that the luminance profile along each raster line varies linearly with the quantity of charge in the successive charge packets. Thus, the FIFO-LIFO mismatch, due to both the propagation delay and to CTI effects, amounts to no more than 6 to 8 percent of the change in luminance between the target and the background. The extent of the mismatch region amounts to no more than about two raster-line spacing along the raster lines. This region extends to the right of the ideal location of each target edge. On the

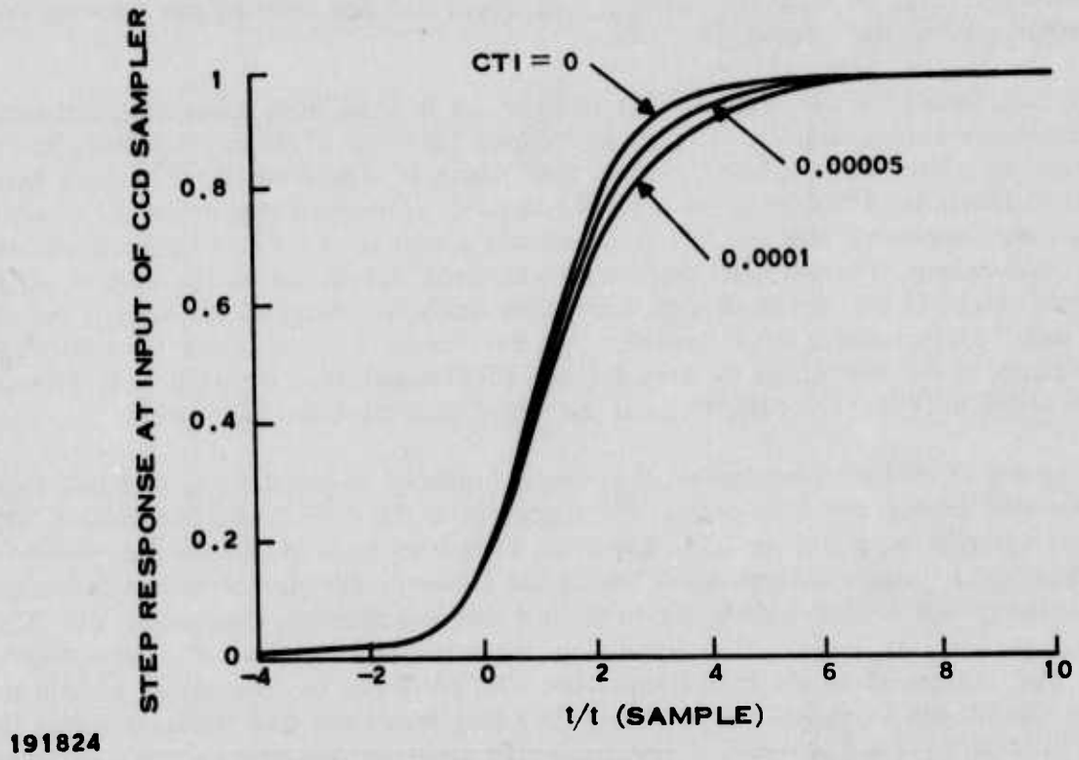

Figure 54. Effect of Charge Transfer Inefficiency on Unit-Step Response

basis of these values, and again considering that they occur over a small angular video, it appears that the overall effects of two-way scan on the detectability of a target will not be significant so long as the CTI is less than 7×10^{-5}.

3. Dark Current

The dark current or what is also referred to as leakage current, is the most pertinent CCD device parameter at this time. Other parameters such as CTE and threshold voltage have influenced the device architecture and, hence, impacted circuit layout and, to a limited extent, system performance. The dark current, however, directly defines the dynamic range of the image buffer module as a function of temperature. This factor then will be the primary one in determining device yield. The purpose of this section is to define the required dark level for the module.

The dark current in the CCD results from the thermal generation of charges within the device both at the surface and within the bulk. The charge is generated at a fixed rate in time at a given location within the device. Since in a three-phase CCD every third electrode is always on, the charge generated in the area of the "on" electrode and its neighboring area will be accumulated under the "on" electrode. This charge adds with the charge under that electrode and ultimately modifies the voltage at the output when that pixel is dumped at the output node. If the amount of charge associated with each pixel were the same, the only effect of the dark current would be to modify the dc level on which the ac video appears at the output of the CCD. Since the postconditioner circuit clamps the output of each CCD to offset variations in the quiescent operating point of the CCDs, the additional variations due to dark current would be of

no consequence. There are, however, two-way scan effects and also noise effects resulting from nonuniformities in the dark-current generation.

The dark current which affects output video occurs in three ways: load, store, and noise. Effects are shown diagrammatically in Figure 55 for both LIFO and FIFO modes. When a line of video from the video chain is being loaded, total length of time from the first pixel being converted to charge until the last pixel is 11.67 milliseconds. Hence, during the period of active load, the charge associated with the first pixel increases according to the dark current integrated over 11.7 milliseconds. The last pixel receives no additional increase during this portion of the "load-dump" cycle. If the sources of dark current are uniform throughout the devices, the net effect is that the signal charge will be modified by a linear ramp. Since the pixels from the FLIR FOV are loaded in different orders for the LIFO and FIFO modes, the ramps will be in different directions within the LIFO and FIFO CCDs at the end of their respective load cycles.

After the CCDs have been loaded, the video information is stored for a minimum time: 3.8 milliseconds. During this store period, the change from the dark current accumulates with that of the signal in the stored pixels. To this point it has been assumed that the dark current is generated uniformly within the area under the device. However, the dark current at each point within the device will have a variance due to the fact that it is thermally generated charge. That variance in the quantity is just the square root of the total. This temporal effect is negligible, however, when compared to the spatial variations. The latter can be observed by loading the CCD very rapidly with a constant charge, storing for a long period and then rapidly dumping the device. The output will not be constant with an additive ramp, but will have an appearance such as indicated in Figure 55. The variance from a straight line will be repetitive for a single device but differs from device to device.

From observations, two types of spatial variations are generally exhibited by CCDs: low frequency and spikes. The spikes result from point defects within the bulk of the material. The fact that the dark current is significantly higher under one electrode than any of its neighbors does not impact the displayed image since the filter in the postconditioner removes elements at the sampling frequency. The low-frequency variations can, however, degrade image quality if not kept to a low value. The origin of these variations is not well understood at this time and the best solution to their presence is to keep the total dark current low since the variance scales with the total value.

The ways in which dark current can impact displayed video have been defined as significant enough to warrant further evaluation of the ramp effect and low-frequency variance. The magnitude of these effects has a strong dependence upon temperature. The dark current itself increases by a factor of 2 for every 8°C increase in the CCD temperature. Hence, if the dark current is rated as 10 nA/cm^2 at 24°C, it will be 160 and 640 nA/cm^2, respectively, for temperatures of 56°C and 72°C. The magnitude of the dark-current effects as a function of 24°C dark current are shown in Figure 56 for 24°C, 56°C and 72°C. Note that the values are given in terms of the fraction of the well that is filled. This can be done since the buried-channel device has a charge storage capability per unit electrode area, and the dark current is also rated per unit area. The examples used are for worst case which is that of electronic magnification. In this example, portions of the information at the lower portion of the display will have been in fixed storage for 35.9 milliseconds.

If the device is rated at 1 nA/cm^2 and the operating temperature is raised to 72°C, the amount of charge due to dark current in the pixel corresponding to the lowermost left-hand side

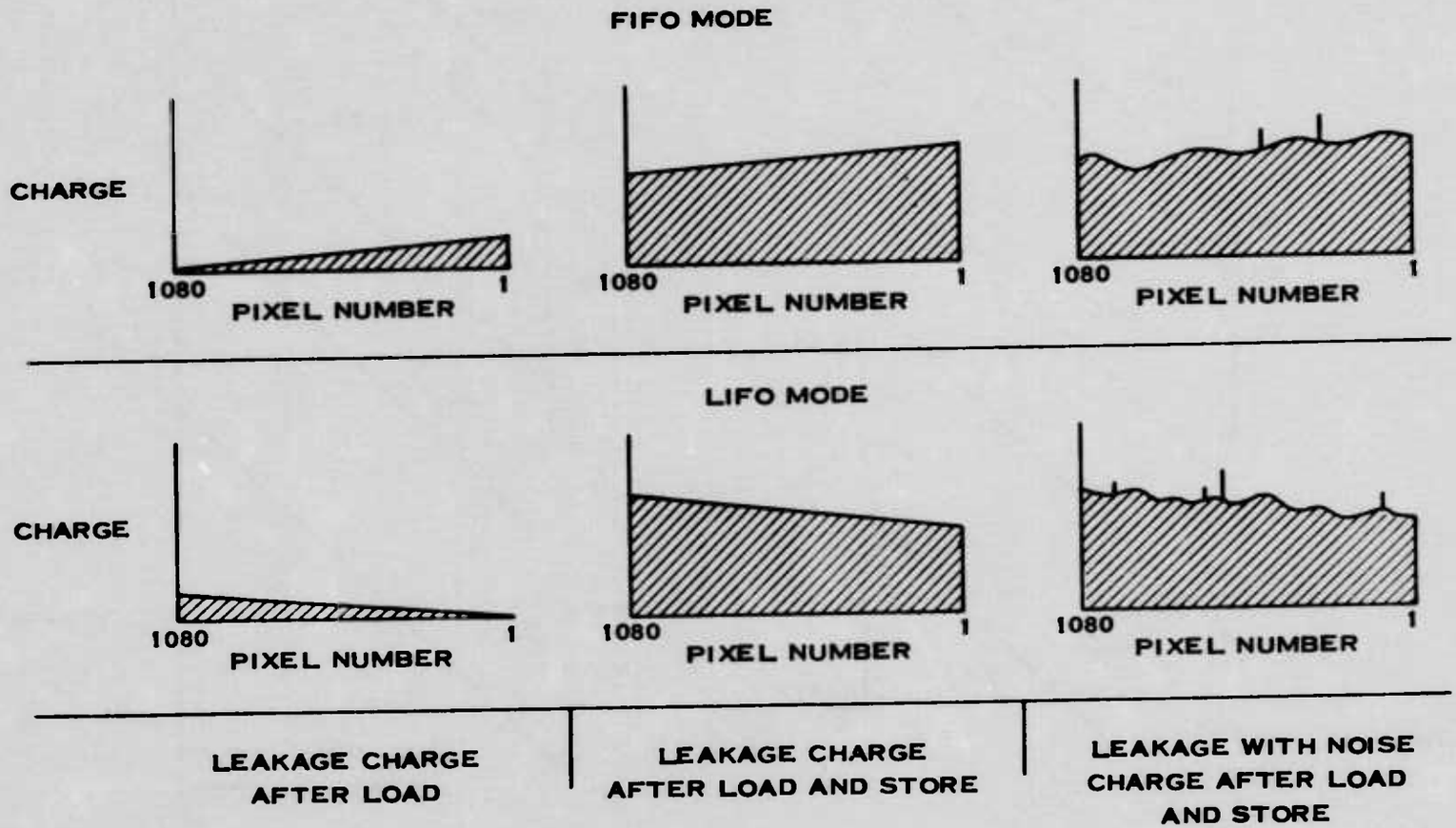

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Figure 55. Dark-Current Effects

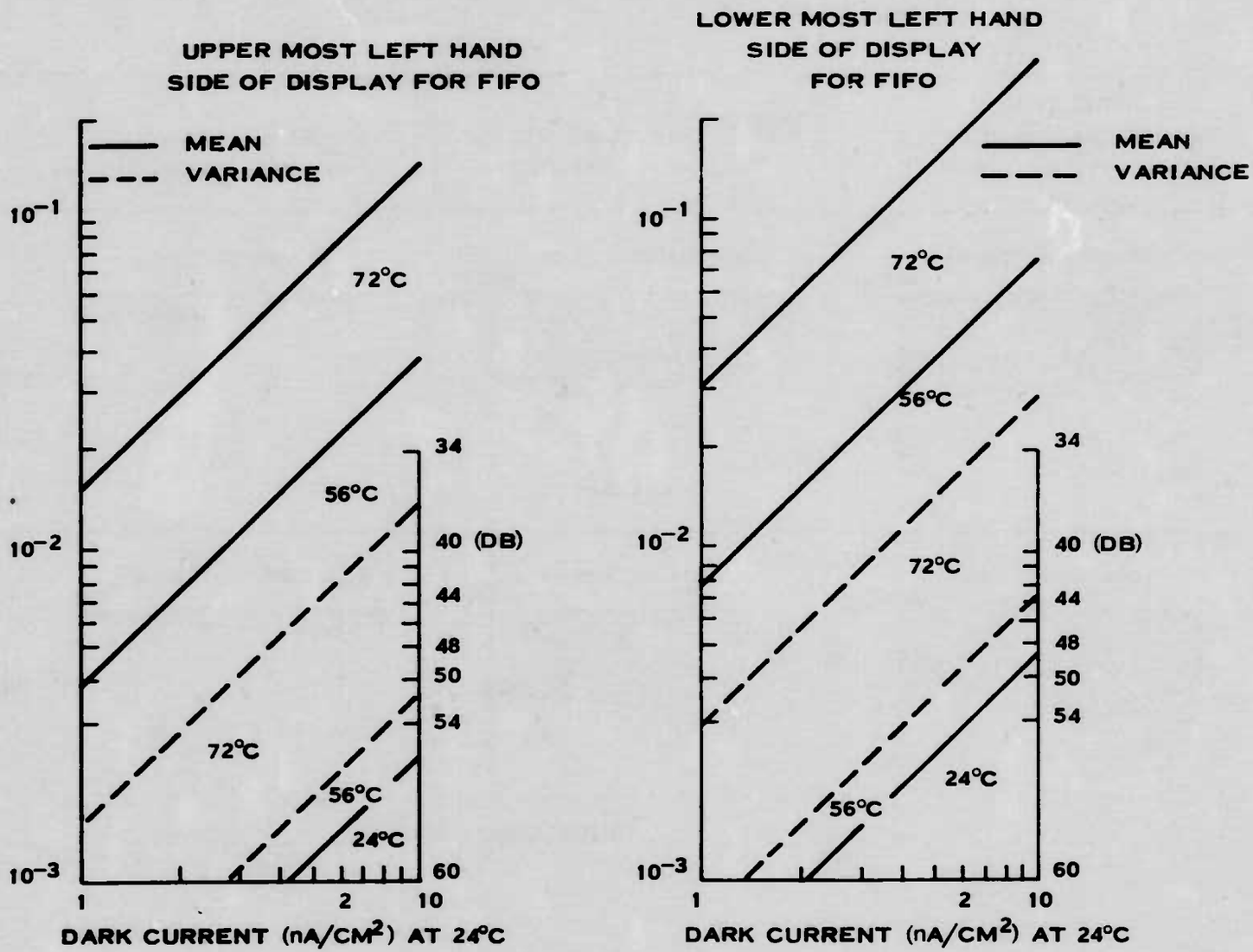

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Figure 56. Fraction of Full Well Filled for System with Electronic Magnification

of the display fills approximately 3 percent of the total usable well. The values for 56°C and 24°C are lower as are those for the upper portion of the display. Dynamic range for the module with devices rated at 1 nA/cm² will depend upon the variance of the total value. As indicated earlier, exact magnitude and frequency of the low-frequency noise is not known. However, it has generally been observed to have a 1 σ value of less than 10 percent of the total value. Hence, as indicated in Figure 56, dynamic range of a system operating at 72°C, containing devices which are rated at 1 nA/cm², will be approximately 50 dB.

Values of 56°C and 72°C are the two temperature values for which systems are usually rated, with the lower value for the higher performance airborne applications. Since CRTs are usually rated at 32-dB dynamic range, the video processor has a higher rating of 40 dB and the image buffer module should have a 43 dB or greater rating. From the figure it is seen that, under the assumptions used here, this can be obtained with a dark-current rating of less than 8 nA/cm² for the 56°C applications but must be improved to 2 nA/cm² for systems in a 72°C ambient air environment. When the dynamic range of the image buffer is reduced by temperature to a value of 44 dB, video into that unit should be optimized to match that of the CRT. This can be done by adjustment of the gain and offset controls on the post-amplifier board presently used on all modular FLIR systems.

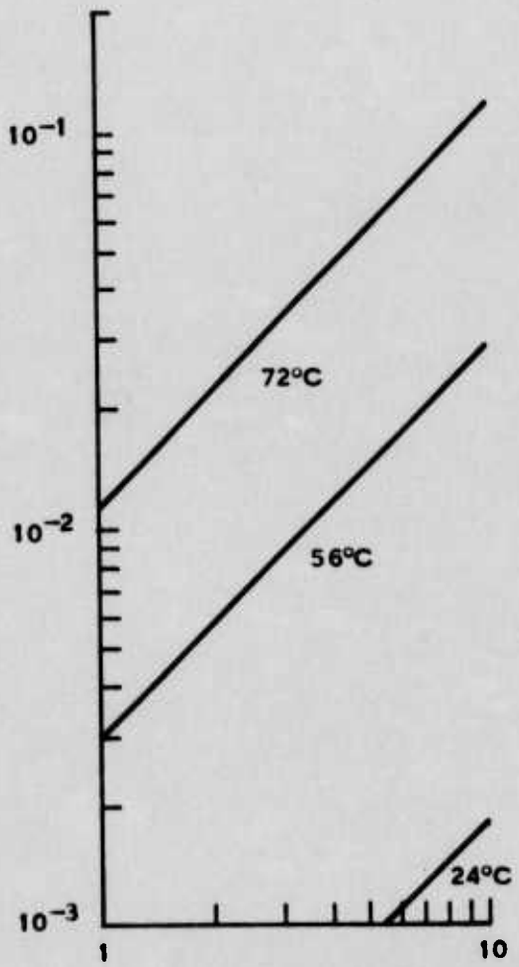

Figure 57. Display Edge Delta From Dark Current

The other factor to be quantified is the effect of the dark current ramp. Since the post-conditioner circuit clamps each line to the quiescent operating point of the CCD, this ramp effect will not be visible on the left of the display. However, on the right side there will be a difference between adjacent CRT raster lines due to the different slopes from the FIFO and LIFO CCDs. The magnitude of this edge difference is shown in Figure 57 as a function of dark current specification at 24°C. Again, excellent performance can be achieved at 56°C operation. Also, the performance is good over most of the display for 72°C. However, for a dark-current rating of 2 nA/cm² and 72°C operation, the error on the information on the right side of the display is just below the minimal required for interface to the CRT.

All results discussed here are summarized in Table 10. As indicated in this table, a CCD dark-current rating of 2 nA/cm² will provide acceptable performance even at operational temperatures of 72°C. Present process ratings are 10 nA/cm² worst case and less than

TABLE 10. DARK CURRENT SYNOPSIS

Dark Current at 24°C ($\mu A/cm^2$)	System Temperature (°C)	Line-To-Line Delta (fraction)	Fraction of Well Filled	Dynamic Range (dB) σ of 0.1	Remarks
1	56	3×10^{-3}	8×10^{-3}	>60	Conditions meet requirements for idealized system
2	56	6×10^{-3}	1.5×10^{-2}	≈56	Acceptable performance with nonuniformity on one edge of display for low-contrast scenes
1	72	1×10^{-2}	3×10^{-2}	≈50	Ideal performance if a variable gain of 20 is used in the post-amplifier
2	72	2.5×10^{-2}	6×10^{-2}	≈44	Acceptable performance if a variable gain of 20 is used in the postamplifier

1 nA/cm^2 for best case. Hence, it is anticipated that initially the operational temperature will affect the device yield and, hence, unit cost. This is discussed further in the section on deployment considerations.

C. COMPONENT SPECIFICATION

The optimum CCD architecture has been defined as the DLM configuration with a total pixel storage capacity of 1080 divided into three registers. This conclusion was based upon control requirements and fixed-pattern noise effects. Image quality was evaluated at the display level using the DLM parameters. Variables in that analysis were clock propagation delays, antialiasing filter characteristics (break frequency), CTE of the DLM and dark current of the DLM. It was shown that the critical design factor was the relative edge responses of adjacent LIFO and FIFO lines. Using edge-response analysis, the result was that all CTE effects will be below the observer perception level if the DLM CCD has CTE of greater than 0.99993.

Gross dark-current effects can be compensated for average device levels of 2.0 nA/cm^2 as measured at 24°C. Dark-current effects upon system dynamic range are, however, more difficult to specify due to a lack of knowledge of the spatial variations of currents within the device area. If is is assumed that the deviation is a factor of 10 below the average value, 2.0 nA/cm^2 is again acceptable. However, if it develops that the variance is higher, the absolute value must be lower.

Within the MOS support circuitry, the source quiescent operating point at the output source follower must be held within ±0.25 volt. Also, the on-chip resistors and capacitors used in the antialiasing filters must have a variance with a given processing run of less than 1 and 5 percent, respectively.

SECTION IX

DEPLOYMENT CONSIDERATIONS

A. COST, WEIGHT, VOLUME AND POWER CONSUMPTION

Module cost is dominated by the hybrid package containing the LIFO CCD, FIFO CCD and the two CMOS clock buffers. The cost of the hybrid is itself dominated by the yield of the devices and the number of packages which must be discarded. For example, cost of the CCDs and CMOS chips may be low, but if the cost of handling the chips and the package itself is high and either the CMOS or CCDs are not usable, the impact on total package yield is significant. This can be seen by analyzing Table 11. To minimize the final package cost, yield at burn-in, Y_{bi}, must be high and the values associated with the package, (PC) and (PL), low. For Y_{bi} to be high the devices which went into the package must all be functional and meet the device specifications. This can best be achieved by performing a more complex analysis at the slice level than is usually done.

TABLE 11. BASIC COST ANALYSIS

C_m = Chip cost for MOS-CCD

$C_m = (S_m/Y_{ms})(1/N_m) + (CSB)$

C_c = Chip cost for CMOS

$C_c = (S_c/Y_{cs})(1/N_c) + (CSB)$

$P = C_m/Y_{sb} + C_c/Y_{sb} + (PC) + (PL)$

B = Cost at functional package level (Burn-in)

$B = P/Y_{bi} + (BL)$

S_m = Processing cost per slice for MOS-CCD

N_m = Number of devices per MOS-CCD slice

Y_{ms} = Yield of MOS-CCD through probe

S_c = Processing cost per slice for CMOS

N_c = Number of devices per CMOS slice

Y_{cs} = Yield of CMOS through probe

CSB = Cost of scribe and break per slice

Y_{sb} = Yield on scribe and break operation and bonding

PC = Cost per carrier

PL = Cost of labor in bonding

Y_{bi} = Yield at burn-in

(BL) = Cost of labor in burn-in

$$B = \frac{\dfrac{\dfrac{S_m}{N_m * Y_{ms}} + \dfrac{S_c}{N_c * Y_{cs}} + 2(CSB)}{Y_{sb}} + (PC) + (PL.)}{Y_{bi}} + (BL.)$$

The key element is Y_{bi}. If Y_{ms} and Y_{cs} do not include functional test, then Y_{bi} contains the product of the two functional yields. This effect significantly modifies B due to (PC) and (PL.).

In present operation, Y_{ms} and Y_{cs} reflect the yield as defined by dc probe, i.e., open and shorts within the device. Items such as dark current, CTE, threshold voltage, and propagation delay are not evaluated until Y_{bi}. The difference in Y_{ms} and Y_{cs}, when probed for functional performance and dc operation, is typically about 70 percent. Hence, one key item in the cost is to perform a full functional probe at the slice level. Another aspect of yield is total active electrode area. The larger the area, the lower the yield, and, similarly, if the area is too small, the handling yield becomes significant. Total electrode area for the final DLM device will be approximately 5×10^3 mils^2 and the CMOS clock drivers will be approximately the same size. Generally, device electrode areas in excess of 10^4 mils^2 are not desirable from the standpoint of yield. Hence, at this time it has not been decided if the individual chip carriers will contain four or two chips. It is certain, however, that the CMOS and MOS-CCD will not be on a single chip.

Volume and weight of the buffer have already been discussed in Subsection V.B. The remaining factor is power consumption. Table 12 contains the best estimate that can be made at present. It is obvious from this table that the memory is itself inconsequential, and that the postconditioner is the primary area for potential improvement. Circuits such as the automatic gain normalization have yet to be fabricated and evaluated. Until this is done, the estimate of the postconditioner must be conservative. Values for power, weight and volume which hold for the case of electronic magnification are given in Table 1 which summarizes these values and compares them to the E-O multiplexer.

TABLE 12. POWER CONSUMPTION WITH ELECTRONIC MAGNIFICATION

	Power (watts)
Controller	
Based on 7 watts for expanded roof-top circuitry and then optimized with CMOS	4.0
CCD	
Based on 180 detector FLIR with 1.33 electronic magnification	
Load	0.6
Dump	0.9
Memory Board Overhead	0.8
Based upon 15 boards for electronic magnification	
Postconditioner	4.0
A very conservative assumption which cannot be checked until detailed design and breadboards tasks completed	
TOTAL	10.3

B. RELIABILITY, MAINTAINABILITY AND SAFETY

At present, data is being accumulated on the failure mechanisms and rate of CCDs. Results on the CCDs are not yet complete, hence this analysis must be based upon similar components rather than exact devices. To date, the only failures in the CCDs were in the output stage where

two opens occurred. This is not a catastrophic failure in that it will not destroy any other device and will appear at the display as a saturated line, either black or white depending upon the polarity of the scene.

If devices of similar nature and complexity are used as a guideline, the failure rate is one per 1.5×10^6 hours for 54°C operation. For a complete memory board this gives one failure every 1.1×10^4 hours at 54°C operation. As further insurance against failure, all memory boards will have surge and spike protection built in. This data, if it holds for the actual CCDs and CMOS devices, will give a satisfactory reliability factor. Maintainability will be straightforward in that cell memory failures will give a solid line at the display. The line can be roughly or accurately determined and either the entire memory board or the particular mother carrier containing that chip carrier will be replaced. Since the automatic gain normalization operation will take only several seconds to perform, the system can be returned to full operation very quickly.

In terms of safety, maximum voltage required by the module is 15 volts, which is currently limited to 10 mA. The 5-volt supply which draws the maximum current will be limited to 0.8 ampere. In addition to limiting each supply, values at each board are also limited for that particular board and all connectors will be resistive to improper plug-in.

SECTION X

SUMMARY AND RECOMMENDATIONS

The CCD Image-Buffer Module has been defined and a CCD architecture, DLM, has been shown to be optimum for the memory element. The performance analysis included display uniformity, MRT and dynamic range. A summary of these considerations and their impact upon the module and device design is given in Table 13. Considerations were also made concerning deployment. These, due to the lack of data in the specific area of CCDs, were somewhat cursory. However, sufficient data is available to show that the buffer concept does provide cost, weight, volume, and power-consumption benefits. These benefits are realizable even when the buffer has an electronic magnification capability. It is recommended that a module based upon the results of this study be designed, fabricated, and evaluated.

TABLE 13. DESIGN CONSIDERATIONS

Item	Solution
Display Uniformity	
DC Offset Compensation	Provide active loads in differential output source follower
Dark Current (two-way scan) Limits	Less than 2 nA/cm^2; Status: less than 1 nA/cm^2
Insertion Loss	Provide automatic gain normalization
MRT	
Horizontal	
Antialiasing Filter	Provide on-chip double RC circuit
Vertical (two-way scan)	
Phase Compensation	Provide delay in LIFO read clocks
CTE	>0.99993 required; Status: >0.99999 with 95 percent >0.9999
Dynamic Range	
Precharge Phase Clock Timing	In-package CMOS clock buffer
Feedthrough of Load Clocks into Dump Signal	CCD layout and differential output
Phase Clock Variance	Single-chip CMOS clock buffer
Dark Current	Spatial Variance <0.2 nA/cm^2; Status: approximately at this point

APPENDIX A
IMAGE ASSESSMENT CRITERIA

APPENDIX A
IMAGE ASSESSMENT CRITERIA

A. IMPULSE RESPONSE FUNCTION

An optical system that is forming an image of an object consisting of a random distribution of point sources will be considered herein. Each point source is imaged into a distribution of intensity in the image plane that is called an impulse response function $I(x,y)$. The lateral extent τ_o of this function is to be determined by evaluating the effective width of the correlation of this function with respect to itself.

First, we assume that the functional dependence of I on x and y is separable, i.e., $I(x,y) = I_x(x)\ I_y(y)$; we further assume that $I_x(x)$ and $I_y(y)$ have the same functional form.

The autocorrelation $C(\tau)$ of $I_x(x)$ with respect to itself displaced by a lateral offset τ is

$$C(\tau) = \int_{-\infty}^{+\infty} I_x(x)\ I_x(x + \tau)\ dx$$

By analogy with the electrical equivalent, the system transfer function for the optical system, i.e., the optical system transfer function $OTF(\omega_x)$, is taken as the Fourier transform of the system impulse response function $I_x(x)$:

$$OTF(\omega_x) = \int_{-\infty}^{+\infty} I_x(x)\ \exp(-jx\omega_x)\ dx$$

The inverse transform has the form

$$I_x(x) = (1/2\ \pi) \int_{-\infty}^{+\infty} OTF(\omega_x)\ \exp(jx\omega_x)\ d\omega_x$$

Thus the autocorrelation function becomes

$$C(\tau) = (1/2\ \pi)^2 \int_{-\infty}^{+\infty} dx \iint_{-\infty}^{+\infty} d\omega_x d\omega_x'\ OTF(\omega_x)\ OTF(\omega_x')$$

$$\exp\left[jx\omega_x + j\omega_x'\ (x + \tau)\right]$$

Now, by the conventional definition of the delta function,

$$\delta(-\omega_x - \omega_x') = (1/2\,\pi) \int_{-\infty}^{+\infty} dx \exp\,[jx(\omega_x + \omega_x')]$$

So

$$C(\tau) = (1/2\pi) \int_{-\infty}^{+\infty} d\omega_x\ OTF(\omega_x) \int_{-\infty}^{+\infty} d\omega_x'\ \exp(j\tau\omega_x)$$

$$\delta\ (-\omega_x - \ _x')$$

$$= (1/2\pi) \int_{-\omega}^{+\infty} d\omega_x\ OTF(\omega_x)\ OTF(-\omega_x)\ \exp(j\tau\omega_x)$$

The amplitude part of the complex OTF is called the modulation transfer function MTF:

$$|OTF(\omega_x)| = MTF\ (\omega_x)$$

So

$$OTF(\omega_x)\ OTF(-\omega_x) = [MTF(\omega_x)]^2$$

and

$$C(\tau) = (1/2\,\pi) \int_{-\infty}^{+\infty} d\omega_x\ [MTF(\omega_x)]^2 \exp(j\tau\omega_x)$$

For $\tau \to 0$,

$$C(0) = (1/2\,\pi) \int_{-m}^{+\infty} d\omega_x\ [MTF(\omega_x)]^2 = \int_{-\infty}^{+\infty} df_x\ [MTF(f_x)]^2$$

We seek to determine the effective value of τ by evaluating the total area under the $C(\tau)$ curve.

$$\int_{-\infty}^{+\infty} d\tau C(\tau) = (1/2\,\pi) \int_{-\infty}^{+\infty} d\omega_x \, [MTF(\omega_x)]^2 \int_{-\infty}^{+\infty} d\tau \, \exp(j\tau\omega_x)$$

$$= \int_{-\infty}^{+\infty} d\omega_x \, [MTF(\omega_x)]^2 \, \delta(-\omega_x)$$

$$= [MTF(0)]^2 = 1$$

The effective width W of the autocorrelation function is just the interval Δx over which there is significant statistical correlation of the impulse response function with itself. This effective width is just the total area under the autocorrelation curve, divided by the peak value C(0).

$$W = [1/C(0)] \int_{-\infty}^{+\infty} d\tau \, C(\tau) = 1/C(0)$$

$$= 1/\int_{-\infty}^{+\infty} df_x \, [MTF(f_x)]^2 = 1/2 \int_{0}^{+\infty} df_x \, [MTF(f_x)]^2$$

since MTF is an even function. This correlation interval is usually defined as r_x, so

$$r_x = 1/2 \int_{-\infty}^{+\infty} df_x \, [MTF(f_x)]^2$$

Hence the farther the MTF curve extends toward high frequencies, the shorter is the correlation width of the associated impulse response function.

B. UNIT-STEP RESPONSE FUNCTION

In this same optical system we now consider the object to be a step function U(x), i.e., a target with a sharp edge located at x = 0 and extending in the y direction. In the image plane there is a distribution E(x) resulting from this. We seek to characterize the narrowness of E(x) by determining its spatial gradient $\partial E(x)/\partial x$ at x = 0.

The superposition principle states that the response E(x) of a linear system to an arbitrary source function f(x) is the convolution of the impulse response function $I_x(x)$ with f(x).

$$E(x) = \int_{-\infty}^{+\infty} d\tau\ f(\tau)\ I_x\ (\tau - x)$$

By the convolution theorem.

$F[E(x)] = F[f(x)]\ F[I_x(x)]$, where F( ) is the Fourier transform. Let f(x) be U(x), the transformation of U(x) to the image plane.

$$U(x) = 1/2 + 1/2\ \mathrm{sgn}(x)$$

By Papoulis, The Fourier Integral, Equation 3-13,

$$F[U(x)] = \pi\delta\ (\omega_x) - j/\omega_x$$

As before, $F[I_x(x)] = OTF(\ _x)$, so

$$F[E(x)] = [\pi\delta(\omega_x) - j/\omega_x]\ OTF\ (\omega_x)$$

The inverse transform is

$$E(x) = (1/2\ \pi) \int_{-\infty}^{+\infty} d\omega_x [\pi\delta(\omega_x) - J/\omega_x]\ OTF(\omega_x)\ \exp\ (jx\omega_x)$$

$$= 1/2 \int_{-\infty}^{+\infty} d\omega_x\ \delta(\omega_x)\ OTF(\omega_x)\ \exp\ (jx\omega_x)$$

$$- (j/2\ ) \int_{-\infty}^{+\infty} d\omega_x\ [OTF(\omega_x)/\omega_x]\ \exp\ (jx\omega_x)$$

Expand $\exp(jx\omega_x)$ in powers of x and get

$$E(x) = 1/2\ OTF(o) - (j/2\pi) \int_{-\infty}^{+\infty} d\omega_x\ [OTF(\omega_x)/\omega_x + jx\ OTF(\omega_x)$$

$$- (x^2/2)\ \omega_x\ OTF(\omega_x) + \text{higher powers of } x$$

$$= 1/2 - j/2\pi \int_{-\infty}^{+\infty} d\omega_x\ OTF(\omega_x)/\omega_x + (x/2\pi) \int_{-\infty}^{+\infty} OTF(\omega_x)$$

$$d\omega_x + \text{higher order terms in } x$$

Now

$$\delta E(x)/\delta x/_{x=o} = m_o = (1/2\ \pi) \int_{-\infty}^{+\infty} OTF(\omega_x)\ d\omega_x = \int_{-\infty}^{+\infty} OTF(f_x)\ df_x$$

If the phase shift associated with the OTF is not large in the range of f_x for which the OTF has significant value, then

$$\int_{-\infty}^{+\infty} OTF(f_x)\ df_x \simeq 2 \int_{0}^{\infty} MTF\ (f_x)\ df_x$$

Thus, as the MTF extends to higher frequencies, the slope of the response function becomes steeper and the vertical edges of a target appear sharper.

APPENDIX B

SNRD AND SYSTEM MTF FOR E/O AND CCD SYSTEMS

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SNRD AND SYSTEM MTF FOR E/O AND CCD SYSTEMS

An observer looking at a target as shown on a TV display perceives a level of noise that is related to the integral of the fluctuation in the brightness level over the entire area of the displayed target. The fluctuations in each line of the display are statistically independent of each other line; they occur at all the frequencies for which noise input are significant and which are passed by the signal channel. The spectral variance $N^2(F)$ of the noise fluctuations at the display as a function of frequency is given by the spectral variance of the noise input, as modified by the MTF of the signal channel extending from the point of noise input to the display.

The observer's eye integrates the perceived noise fluctuations over the entire area of the displayed target and over a moving time interval of about 0.2 sec., which approximates the persistence function of the eye. The integration of the noise variance over the eye integration time T_e and over the vertical subtense H_t of the target yields the factors $\frac{T_e}{T_f}\frac{H_t}{\Delta\theta_y}$, where T_e/T_f is the number of display-frame periods per eye integration time, i.e., about 6, and $\Delta\theta_y$ is the vertical angular subtense of an individual FLIR detector. The integration over the horizontal subtense W_t of the target gives the term

$$\left(\frac{W_t}{\Delta\theta_x}\ T_d\right)^2 \int_0^\infty N^2(F)\ \mathrm{sinc}^2\left(\pi F/2F_t\right) dF$$

where $\Delta\theta_x$ is the horizontal subtense of a detector. Here T_d is the equivalent dwell time of the FLIR scan on a detector width $\Delta\theta_x$, i.e., $T_d = \Delta\theta_x/V_s$, where V_s is the scan speed. The horizontal term arises from the integration over the width W_t. F_t is the fundamental frequency of a target of width W_t, given by $F_t = 1/2\ T_t = V_s/2W_t$, where T_t is the scan time across the target width.

The integral term can be normalized with respect to the target fundamental frequency as follows:

$$\left(\frac{W_t}{\Delta\theta_x}\ T_d\right)^2\ F_t\left[\frac{1}{F_t}\int_0^\infty N^2(F)\ \mathrm{sinc}^2\left(\pi F/2F_t\right) dF\right]$$

For most FLIR systems, the detector noise is the dominant component of the displayed noise. Thus $N^2(F) = G(F)\, a^2(F)$, where $G(F)$ is the spectral noise variance of the detector, and $a(F)$ is the product of the transfer functions of all the signal channel components after the detector.

The detector noise variance can be related to the detector noise equivalent temperature NET. Define a relative noise spectral function $g(F) = G(F)/\overline{G}$, where $\overline{G}$ is some mean value of the detector noise variance. Then NET can be expressed in terms of G and the system fundamental frequency $F_o = 1/2\ T_d = V_s/2\Delta\theta_x$:

$$(NET)^2 = \overline{G}\, F_o$$

So

$$G(F) = g(F)(NET)^2/F_o$$

and

$$N^2(F) = g(F)\, a^2(F)(NET)^2/F_o$$

Thus the horizontal term becomes

$$\left(\frac{W_t}{\Delta\theta_x}\ T_d\right)\ \frac{F_t}{F_o}\ (NET)^2\ \left[\frac{1}{F_t}\int_o^\infty \cdots\right]$$

Use the relation $F_t/F_o = \Delta\theta_x/W_t$ and get the final expression for the noise variance integrated over the entire area of the target:

$$N^2 = \frac{T_e}{T_f}\,\frac{H_t}{\Delta\theta_y}\,\frac{W_t}{\Delta\theta_x}\,T_d^2\ (NET)^2\left[\frac{1}{F_t}\int_o^\infty g(F)\ a^2(F)\ \mathrm{sinc}^2\left(\pi F/2F_t\right)\,dF\right]$$

In the image-buffered FLIR, the progress of the detector noise along the signal channel is interrupted by the sampling of the signal at the input to the image buffer. The integral over all frequencies is cut off at 1/2 the sampling frequency F_s, and the higher-frequency components of the detector noise are folded back into the frequency range below $F_s/2$. Let the total system transfer function $a(F)$ be divided into a $a_1(F)$, associated with all the components between the detector output and the image buffer input, and $a_2(F)$, representing

all the subsequent components. The the noise spectral variance at the sampler is $E^2(F)\ \ g(F)\ a_1^2(F)$. The integrated noise power now has the form

$$N^2 = \ldots \left[\frac{1}{F_t}\int_0^{F_s/2} a_2^2(F)\left\{\sum_0^{\infty} E^2\left(F \pm nF_s\right)\right\} \operatorname{sinc}^2\left(\pi F/2F_t\right) dF\right]$$

Here the summation to $+\infty$ replaces the integration to $+\infty$.

The strength of the signal corresponding to the total target, as perceived by the observer, involves similar integration over the horizontal and vertical subtense of the target image and over the eye-persistence time. Since the target is perceived coherently, the eye integration is performed on the signal amplitude; the noise, conversely, is incoherent, so the integration is performed on the variance of the noise. Thus the integrated signal amplitude is given by

$$S = \left[\frac{T_e}{T_f}\frac{H_t}{\Delta\theta_y}\frac{W_t}{\Delta\theta_x}T_d\right]\Delta T_o\ F(SAR)$$

Here the [ ] term is the total dwell time of the scan over the target during the eye integration time, ΔT_o is the effective temperature contrast between the target and its background, and F(SAR) is the system amplitude response function. For an isolated 2-dimensional target that is large in both dimensions relative to the impulse width of the system, F(SAR) = 1. Thus the perceived signal/noise for the target at the display is

$$SNRD_t = \frac{\Delta T_o}{NET}\left[\frac{T_e}{T_f}\frac{H_t}{\Delta\theta_y}\frac{W_t}{\Delta\theta_x}\right]^{1/2} \cdot$$

$$\left\{\frac{1}{T_t}\int_0^{F_s/2} a_2^2(F)\left[\sum_0^{\infty} E^2(F \pm nF_s)\right] \operatorname{sinc}^2\left(\pi F/2F_t\right) dF\right\}^{-1/2}$$

To help suppress the folding back (aliasing) of high-frequency noise into the low frequency range, we introduce an additional low-pass anti-aliasing filter ahead of the sampler. The impact of this on the system MTF is compensated

for by adding a peaking amplifier in the video output circuit, that offsets the attenuation of the anti-aliasing filter ahead of the sampler. The impact of this on the system MTF is compensated for by adding a peaking amplifier in the video output circuit, that offsets the attenuation of the anti-aliasing. As long as the maximum value of the compensatory gain is not too high, the SNRD is not significantly affected, so the net effect is as if the anti-aliasing filter were not there.

The form for the SNRD for an image-buffered system is compared with the corresponding form for an electro-optically multiplexed system, which does not make use of sampling.

$$\frac{\text{SNRD (Image Buffer)}}{\text{SNRD (E/O)}} = \frac{\text{MTF (anti-aliasing) MTF (CCD) MTF (peaking amp)}}{\text{MTF (LED) MTF (TV camera and lens)}}$$

$$\left[\frac{\int_0^{\infty} g(F)\ a^2(F)\ \text{sinc}^2\left(\pi F/2F_t\right) dF}{\int_0^{F_s/2} a_2^2(F) \left\{ \sum_0^{\infty} E^2(F \pm nF_s) \right\} \text{sinc}^2\left(\pi F/2F_t\right) dF} \right]^{1/2}$$

where

$a(F)$ = MTF (pre-amp, post-amp, LED, visible optics, TV camera and lens, CRT)

$a_2(F)$ = MTF (CCD, peaking amp, CRT)

$E^2(F) = g(F)\ a_1^2(F)$

$a_1(F)$ = MTF (pre-amp, anti-aliasing)